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Demand Side Management of Electrical Grids Using Smart Domestic Water Heater Controller

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Declaration of Authorship

I, Farzeen Faiz Adi Rajah, declare that this thesis titled,"Demand Side Management of Electrical Grids Using Smart Domestic Water Heater Controller" and the work presented in it are my own. I confirm that:

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- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
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Abstract

Conventional sources like wind, solar and geothermal energy are available abundantly in New Zealand. These can be put to use to reduce the dependency on conventional sources. In the present, power systems engineers are trying to incorporate more renewable sources into the grid. Due to the intermittent nature of many renewable resources, some control has to be implemented to stabilize the system. This thesis report is a document describing the development of a controller for a domestic water heater, which enables the use of the water heater as a reserve to maintain grid performance.

The controller modulates hot water heating element power which could help stabilize a grid and minimize transport of energy. The controller takes into account the voltage and frequency as grid parameters and determines how much power has to be given to the heating element so that it doesn't load the grid at the peak time, but also provides hot water to the user all the time.

The details of controller specification, design of electrical circuit, PCB design and mechanical design are discussed in this thesis. The testing of the developed controller and modifications required are also presented.

Acknowledgments

I would like to express my most sincere gratitude for the academic guidance and inspiring discussions my supervisor Dr. Alan Wood has provided me throughout my academic career. This thesis cannot be completed without Alan's encouragement and support. His approach to students has been nothing but helpful, and the speed he derive at a clear feasible solution never ceased to amaze me. Thank you very much, Alan.

I would also like to show my appreciation for technical staff of University of Canterbury, Mr Edsel Villa, Mr Michael Cusdin and Mr David Healy for providing me with advice and showing me the practical consideration in the equipment making process when I was building my device. Their knowledge has made the experience much more efficient and enjoyable. Non of this would be possible without the opportunity and the guidance they have offered. I have greatly enjoyed working with laboratory equipment and the value of the work experience has been immeasurable to me.

Finally, I would like to thank my parents for their love and support, and all my postgraduate collegues for maintaining the office environment full of novel ideas and interesting discussions.

Contents

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Symbols

EMF	Electro-Motive Force
AVR	Automatic Voltage Control
EHV	Extra High Voltage
UHV	Ultra High Voltage
kVA	Kilo-Volt-Ampere
FACT	Flexible Alternating Current Transmission System
AC	Alternating Current
TCR	Thyristor-controlled reactor
TSR	Thyristor-switched reactor
TSC	Thyristor-switched capacitor
MSC	Mechanically-switched capacitor
STATCOM	Static synchronous compensator
CE	Contingent Event
SR	spinning reserve
IR	instantaneous reserve
FIR	Fast Instantaneous Reserve
SIR	Sustained Instantaneous reserve
AUFLS	Automatic Under Frequency Load Shedding
ECE	Extended Contingency Events
HVDC	High Voltage Direct Current
SDWHC	Smart Domestic Water Heater Controller
PWM	Pulse Width Modutation
RMS	Root-Mean Square
DCF	Duty Cycle with respect to Frequency
DCV	Duty Cycle with respect to Voltage
DC	Direct Current
D	Duty cycle
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Ellect Transistor
IGBT	Insulated Gate Bipolar Transistor
HF	High Frequency
SMPS	Switched Mode Power Supply
NZD	New Zealand Dollar

SMD	Surface Mount Devices
PCB	Printed Circuit Board
DSP	Digital Signal Processor
LPF	Low Pass Filter
EMI	Electro Magnetic Induction
LCD	Liquid Crystal Display
RDC	Rectifier Discontinuous Conduction

For/Dedicated to/To my...

Chapter 1

Introduction

1.1 Project Introduction

Humankind has made maximum use of the resources available on Earth to suit our comforts and needs. However in this process, we have forgotten to realize that today's wastage is tomorrow's shortage. This has resulted in a very serious problem, namely the Energy and Environmental Crisis. The energy crisis is of great concern today, since the natural resources available in the world are diminishing as the world's demand on them rises and the capacity of the world's atmosphere to absorb increasing CO_2 emissions is limited. These resources though naturally available are of limited supply; it can take hundreds of years to replenish their stores. The crisis is something that is ongoing and getting worse despite many efforts. The reason for this is that there is not a broad understanding of the complex causes and the solutions for the crisis, including issues such as global warming. This research is based on electrical and electronic engineering, specifically, renewable energy and sustainable engineering. The research mainly focuses on renewable energy, which is a partial solution for one of the major issues today due to environmental concerns and excessive depletion of conventional resources.

Energy is a major member in the list of resources without which our existence would be tough. The need for energy has been going up rapidly over the years. The increase in population and continuing industrialisation will increase demand for energy in the future. Due to the these reasons we have to include more non-conventional sources of energy in daily use. In electrical supply networks, monitoring and control must be implemented in the existing grids so as to enable the incorporation of non-conventional sources.

Devices that enable incorporation of the non-conventional sources must be able to compensate the problems that non-conventional sources can cause. There are two significant problems that are partially addressed by this work, both associated with the vaiablity of renewable generation. The first is frequency variation, which arises from an imbalance

between generation and load. Highly variable renewable generation will increase this imbalance. The second is voltage magnitude variation. This is a local problem, where high levels of renewable power generation can cause over-voltage possibly causing damage to local equipment. This research proposes a controller for domestic water heaters that can regulate load in a way that enables variable energy generation to be installed and fully utilized. In this way the variability of renewable generation can be compensated for through controlled variability of load.

1.2 How The Report Is Structured

1. **Chapter 2 - Background**
   This chapter contains an overview of electrical power systems(EPS), their operation and energy storage systems. Various system parameters and controls such as voltage control and frequency control are discussed.

2. **Chapter 3 - Technical Specification**
   The technical requirements of the proposed controller are discussed. This section also covers the New Zealand standards to be met for domestic water heaters.

3. **Chapter 4 - System Modeling**
   The initial development of the system is discussed. Controller topology, switching sequence pattern and determination of switching frequency are also determined.

4. **Chapter 5 - Circuit Implementation**
   This chapter deals with design and implementation of control circuitry, logical algorithm and selection of the process controller.

5. **Chapter 6 - Mechanical Design**
   This chapter mainly discusses the power dissipation in power converters and the heatsink requirements. The guidelines to be followed while designing PCB are also discussed.

6. **Chapter 7 - Circuit Testing**
   Testing of circuits and testing methodology are discussed in this chapter. The results obtained and various waveforms obtained during testing are shown.

7. **Chapter 8 - Conclusion**
   In this chapter the results obtained during testing along with New Zealand power consumption data are mentioned. The overall summary and future prospects of this project are also mentioned.

Chapter 2

Background

2.1 Overview

Renewable resources like wind, solar and geothermal energy are abundantly available in New Zealand. These can be put into use to reduce the dependency on conventional sources. However, the use of these sources comes with its own drawbacks. Wind and solar energy are not reliable as primary sources of energy due to their intermittent nature. These add to the burden on the existing grid. Communication is now being incorporated along with power lines to communicate data like energy demand, production rate and pricing details. Controls like SCADA and distributed control system (DCS) are being employed in the system protection. Problems like islanding, harmonics and frequency control are concerns related with intermittent sources of energy. Research is being conducted to analyse the pattern of energy demand and ways to reduce the effect of intermittent generation. At present, devices like smart meters and solar inverters are being used for managing energy consumption and energy generation patterns respectively. This research involves the development of a controller which could use the domestic water heating load to contribute to stabilisation of grid frequency and local voltage levels.

2.1.1 Smart Grid

A smart grid is a modernized electrical grid that uses information and communications technology to gather and act on information, such as information about the behaviors of suppliers and consumers, in an automated fashion to improve the efficiency, reliability, economics, and sustainability of the production and distribution of electricity[1].

Making the grid more efficient by using the tools, technologies and technique available is the main goal of smart grid[1].

1. Ensuring reliablity to degrees ever before possible.

2. Maintaining its affordability.
3. Reinforcing our global competitiveness.
4. Fully accommodating renewable and traditional energy sources.
5. Potentially reducing our carbon footprint.
6. Introducing advancements and efficiencies yet to be envisioned.

Figure 2.1 shows the representation of the evolution of the grid. It can be seen that in the past system is one sided, i.e the generating stations generate as load consumes power. There is not much communication in between. In future the system is going to be bidirectional with more distributed power sources.

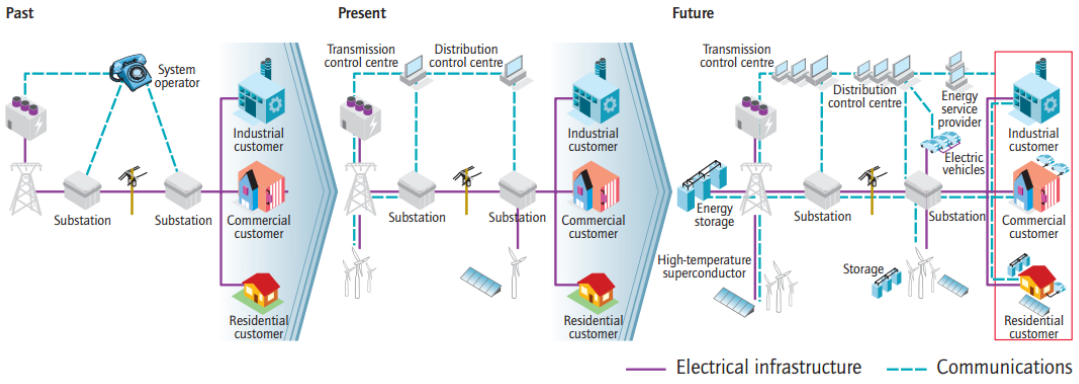


FIGURE 2.1: Overview of present and future grids[2].

2.1.2 Grid voltage regulation using power electronics

Power electronics can be used to help utilities adapt to the rapid increase in distributed residential/commercial solar power generation. Traditional electromechanical systems such as capacitor banks or voltage regulators at substations can take minutes to adjust voltage and can be distant from the solar installations where the problems originate[3]. Voltage on a neighborhood circuit can endanger utility crews and cause damage to utility and customer equipment if it goes too high. A grid fault causes immediate shut-down of the photovoltaic generators. As compared to numerous consumer devices, smart grid based regulators are more controllable. These can also help in power quality. However, the need for expensive utility equipment could be minimised by utilization of modern solar inverters with grid interactive control feactures. Already many electrical standards require grid interactivity such as remote control capablity, Volt-VAR modes and volt-watt modes.

2.2 Voltage Control

The control of voltage and reactive power is a major issue in power system operation[4]. In order to maintain the voltage between regulatory limits there are many voltage control methods employed. The control methods differ depending on where the voltage control is used in the power system. There are various bus in a power systems, generating station bus, switching substation bus, receiving substation buses and distribution substation buses in which the voltage has to be maintained at all times for proper operation of grid. The voltage control methods are as follows:

2.2.1 Excitation Control and Voltage Regulation

The excitation current is the key factor for maintaining the induced EMF of synchronous generators which is achieved by automatic voltage regulation (AVR) system in the generator. These systems are responsible for steady state operation and voltage regulation during faults. The excitation level also defines the extent of reactive power sharing, which helps to maintain the terminal voltage of the generator within limits.

2.2.2 Tap Changing Transformers

Voltage control can also be achieved by changing the turns ratio of transformer through taps. This control method is employed in transmission and distribution system. A voltage control of range $\pm 15\%$ can be acheived by tap changing transformers[5]. There are two types of tap changing:

1. **Off load tap changing** :- These are usually used where there are seasonal load variations. Here the tap changing is done after cutting off the load on the transformer.

2. **On load tap changing** :- This technology is used where the voltage regulation is required with out cutting off the load. These are used where the load pattern vary significantly within a day.

2.2.3 Shunt Reactors

In long EHV and UHV transmission lines, during low load or no load the receiving end voltage will be higher than the sending end voltage. This is because of shunt capacitance of these lines and an effect known as the Ferranti effect. In order to compensate for

the effect, long transmisson lines are provided with shunt reactors at the sending and receiving ends.

2.2.4 Shunt Capacitors

During high load the power factor drops near industrial load due to the inductive loads. The voltage drop due to current I and inductive reactance X_L (IX_L) increases with increase in load. In order to compensate for the drop shunt capacitors are connected near the load centers. The KVA loading on the transformers in substations is reduced by shunt capacitors as they provide leading VAR, which also improve voltage regulation. The capacitor also helps in reduction of harmonics which improves the performance of the system[6].

2.2.5 FACTs Devices

Conventional methods of voltage control, power flow and stability cannot be achieved in extra long high power transmission lines due to the high series reactance. Flexible AC Transmission devices are used in substations in the transmission network. These enable the interconnection of power systems. Some FACTs devices are shown in Figure 2.2.

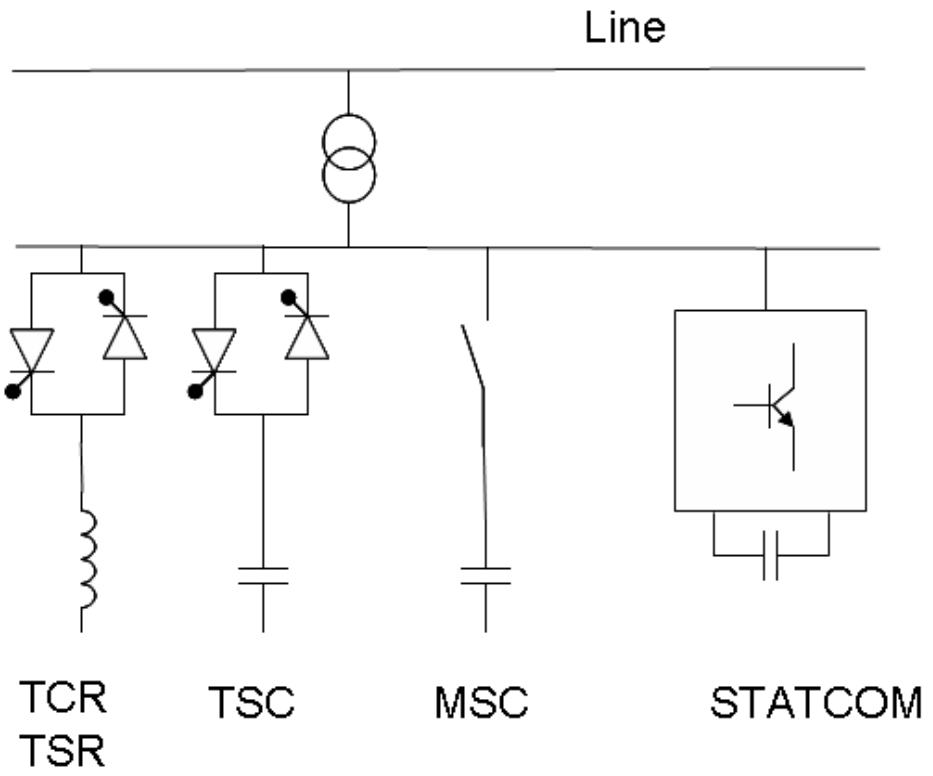


FIGURE 2.2: FACTs devices in shunt configuration [7].

Where	TCR	Thyristor-controlled reactor
	TSR	Thyristor-switched reactor
	TSC	Thyristor-switched capacitor
	MSC	Mechanically-switched capacitor
	STATCOM	Static synchronous compensator

2.3 Frequency Control

Supply quality and security can be improved by frequency stabilisation. Fluctuation in frequency is primarily due to the momentary imbalance in generation and demand of power. Rising system frequency indicates that the generation is greater than demand and vice-versa. Frequency changes according to the changing demand as generation cannot instantaneously match to the demand.

Frequency control aims to bring the difference between supply and demand to zero. Since there is uncertainty in demand forecasting, frequency control is achieved by ensuring that there is sufficient quantity of spinning reserve generation and by slope control. The frequency response of this generation is provided by altering the output according to the system frequency.

2.3.1 Slope Control

The power requirement in a electrical grid is not stable. The generating stations have to respond to the varying requirement moment by moment. Frequency is the main parameter which helps in maintaining the balance. If the grid frequency is increasing then there is excess generation whereas if the frequency is decreasing, the generation is less than demand.

The kinetic energy stored in the large rotating masses is a part of grid inertia[8]. When the load on the system increases, it is met by the grid inertia. This reduces the kinetic energy stored in the turbine. Since the electrical power output is proportional to the mechanical power, the frequency drops as the speed of the turbine decreases. To maintain the frequency more mechanical power is given to the turbine, i.e more water is fed in case of hydro power station or more steam in case of a thermal power station.

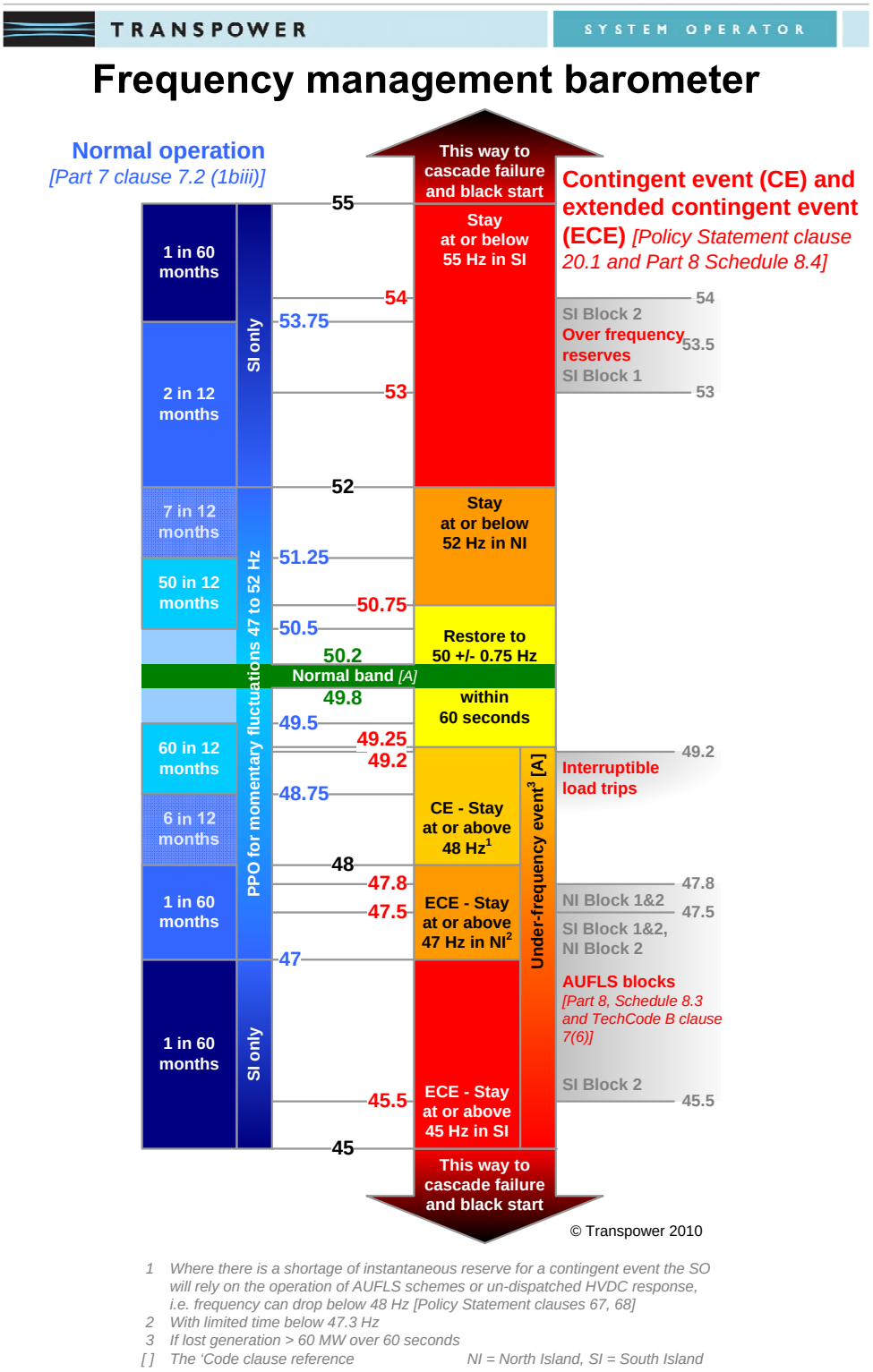


FIGURE 2.3: Frequency range of New Zealand grid[9].

2.3.2 Inertial Control

In a power system the synchronous generators are large rotating machines with large inertia. The stored mechanical energy (inertia) is coupled together in an interconnected system. Imbalances between power generation and demand on a synchronous power system are manifested as a change in system frequency and the stored kinetic energy changes in response to the frequency change[10].

A threat due to integration of more wind and gas turbines is that the system inertia is getting low in New Zealand. When a large generator is lost within a low inertia system, the frequency will fall significantly faster than in a system with higher inertial response[11]. This is a major threat as New Zealand is aiming for 90% renewable energy grid by 2025[12].

2.3.3 Reserves

One of the key parts of demand response in power system is reserves. Reserves can be mainly classified as spinning reserve (SR) and instantaneous reserve (IR). IR is the load that can be shed for demand reduction whereas SR is additional generation capacity that can be made quickly available[13]. IR, based on the time of response can be further classified into Fast Instantaneous Reserve (FIR - arrests frequency fall) and Sustained Instantaneous Reserve (SIR - restores frequency). FIR is the load that can be shed or generation brought online with in 1 second and can be sustained for 60 seconds when system frequency falls below 49.2Hz[14]. SIR is the load that can be shed or generation that can be brought online in first 60 second of grid frequency falling below 49.2Hz[14]. Both SIR and FIR respond when the largest single supply asset trips (risk setter), which helps maintaining the system frequency to avoid cascade failure[15]. The variation in system frequency and activation of IR is shown in Figure 2.4.

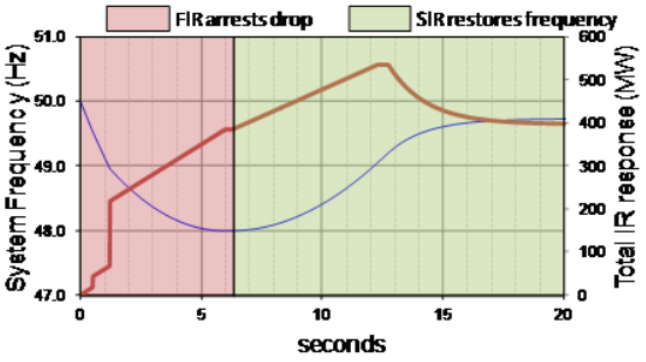


FIGURE 2.4: IR activation chart.[13].

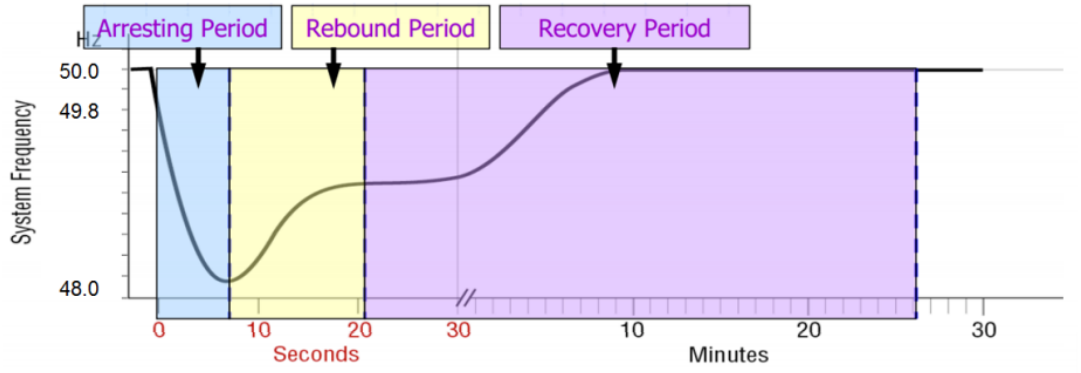


FIGURE 2.5: Typical frequency trace during under frequency event[10].

2.3.4 AUFLS

Automatic Under Frequency Load Shedding is a demand response employed in case of extended contingency events (ECE). ECE is defined as loss of multiple generators or as loss of both HVDC poles[11]. In this system there are loads connected to grid by using under-frequency relays which are shed during ECE. In New Zealand, presently there are two blocks of AUFLS at each grid exit point[10]. The disconnect points are mentioned in Table 2.1.

TABLE 2.1: System parameters defined for AUFLS[10]

Block	Region	Response Time (Second)	Minimum Frequency (Hz)
Block 1	North Island	0.4	47.8
	South Island	0.4	47.5
Block 2	North Island	15	47.8
		0.4	47.5
	South Island	15	47.5
		0.4	45.5

2.4 Domestic Water Heating

In New Zealand water heating is the major component in house energy consumption. 30% of the house energy consumption is by water heating (EECA, 2000). Use of electricity for water heating is the most common with 91% of the homes which utilize 8% of the total energy consumed[16]. According to a BRANZ report normal hot water rating in New Zealand modern homes have one 2kW or 3kW element[17]. According to 1996 census data 88% of New Zealand homes use electricty for water heating and 8% natural gas.

A standard electric storage water heater consumes about 4.82kWhday along with a standing loss of 3.56kWhday which is required by the heater to maintain the temperature[16]. Figure 2.6 shows a typical daily energy use profile for water heating energy use in a house.

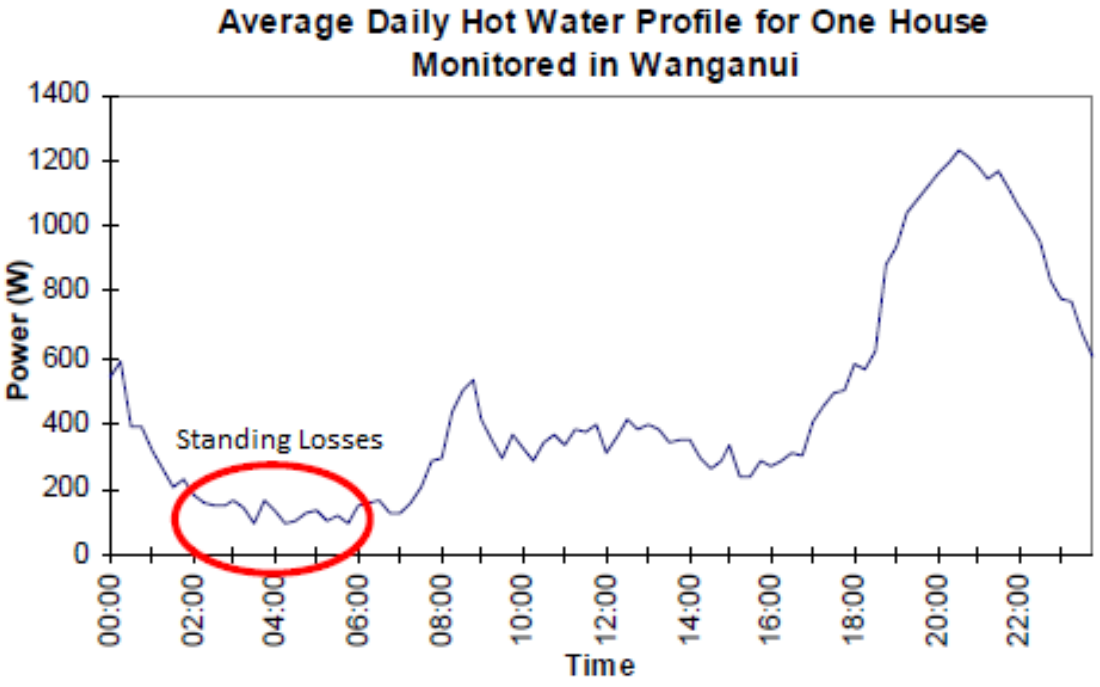


FIGURE 2.6: Typical domestic hot water energy use pattern[16].

Distribution companies in New Zealand use the hot water heater for demand response which is known as ripple control. In order to sucessfully utilize the generation, transmission and distribution assets, ripple control is used to shed the hot water load[15][18]. Figure 2.7 shows a block diagram representation of the ripple control mechanism which is being used.

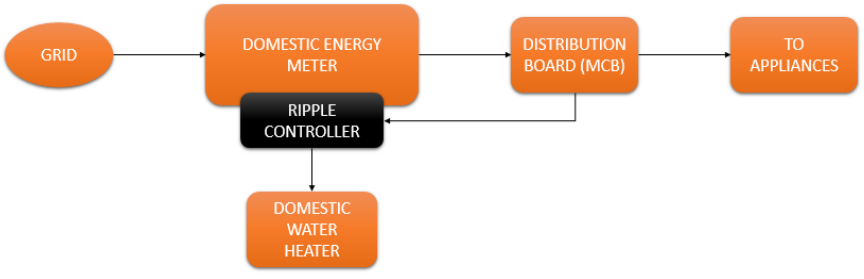


FIGURE 2.7: Present connection of domestic water heater.

This report proposes a Smart Domestic Water Heater Controller (SDWHC) that responds to grid conditions (voltage, frequency and ripple control) and modulates the element power accordingly. Slope control, inertia control and FIR can all be implemented with such a system. The SDWHC is a device which acts as an interface between

the ripple controller and water heater element. The SDWHC directly measures the grid parameters as well as the temperature of the water in the heater. The block diagram representation of the interfacing is shown in Figure 2.8.

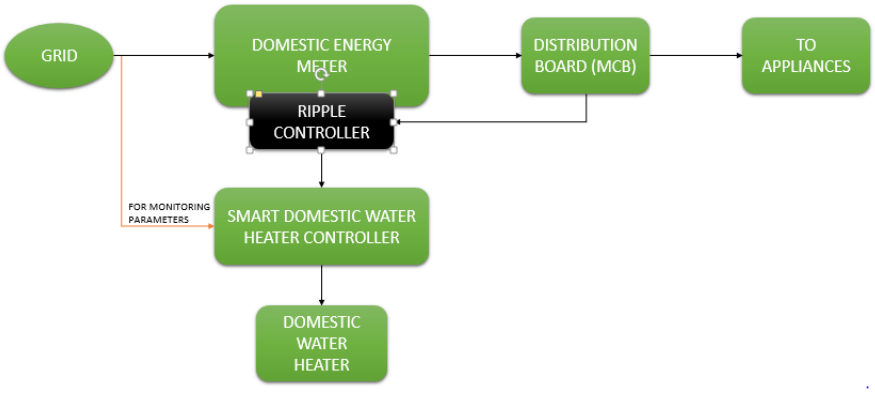


FIGURE 2.8: Interfacing of smart domestic water heater to present system.

According to the 2013 Census[19] there are 1,570,695 occupied dwellings in New Zealand. 8.7% of the dwellings are multi story buildings which have central water heating equipment. This leaves 1,434,044 dwellings using individual domestic hot water systems. BRANZ[20] state that 79.2% of the households use electricity for heating purposes which gives round 1,140,000 dwellings. The average power of a hot water heater is 1.5kW [16]. From Figure 2.6 it can be noted that the domestic heater works at full power only for 4-6 hours a day to cover water usage and standing loss.

Average power consumption during the remaining time to maintain the temperature is 200W (with reference to Figure 2.6). Since this load is available through out the day, with 1,135,763 dwellings the minimum load available for shedding is 227MW. At peak times the load available for control could be as high as the net connected load, i.e 1.704GW (at full load).

By use of the proposed SDWHC, the above calculated load could contribute to frequency keeping, FIR and SIR.

Chapter 3

Technical Specification

3.1 Overview

Before any device or system can be designed or integrated to the power system it has to meet certain functional specification and standards. There are many guidelines and regulations to be followed. This chapter describes the various system requirements.

3.2 System Description

The main idea behind the SDHWC is to develop an interface between the grid and water heater element which regulates the power flow to the heater element. The controller measures the grid parameters (voltage and frequency) in real time and analyses the grid status with respect to the reference parameters, which can be programmed in to the controller.

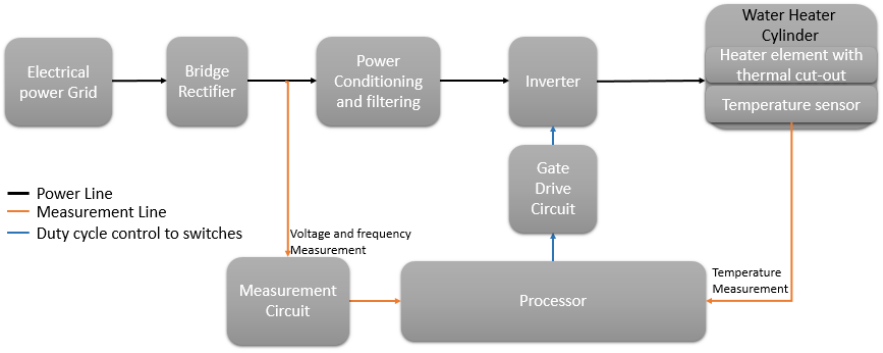


FIGURE 3.1: Detailed block diagram of SDWHC.

Figure 3.1 shows the detailed block diagram of the SDWHC. It consists of a rectifying element, power conditioner, inverter and a processor. The processor measures the grid parameters via the measurement circuit and then determines the duty cycle. The PWM signal is given to inverter switches through a gate drive circuit. The detailed design is discussed in the later chapters.

3.3 System Requirement

1. Electrical Requirement

Parameter	Requirement	Description
Power rating	3 kW	Typical maximum hot water element rating.
Voltage rating [21]	230V, 50Hz	Voltage maintained by distribution companies. Subject to change of ± 6%.
Current rating	15 Amp	

2. Thermostat Requirement :- The thermostat should be adjustable[22].

Parameter	Requirement	Description
Lower limit (LT)	40°C ≤ LT ≤ 50°C	Under normal operation the temperature is maintained at a minimum of 45°C (Manufacturer setting).
Upper limit (UT)	60°C≤ UT ≤ 80°C	

* The thermostat should be able to make changes in steps of 5°C.
* Sensor should be able to detect ± 0.5°C[22].
* Frequency of supply across the thermal-cutout should have fundamental frequency of 50Hz for proper functioning.

3. Electromagnetic Requirement[23]

Harmonic order (n)	Maximum permissible harmonic current (A)
Odd Harmonics	
3	2.3
5	1.14
7	0.77
9	0.40
11	0.33
15 ≤ n ≤q 39	0.15 $\frac{15}{n}$
Even Harmonics	
2	1.08
4	0.43
6	0.30
8 ≤ n ≤ 40	0.23 $\frac{8}{n}$

TABLE 3.1: Harmonic current limits for class A equipment[23]

⇒ Only symmetric power conversion methods are allowed.

⇒ Harmonics during the first 60 seconds of turn ON and OFF can be neglected.

4. Processor Requirement

Measured Parameter	Requirement	Description
Voltage (RMS)	Sampling at rate of 1 sample every 0.05 second	The average of 10 samples is taken for precision.
Frequency	Maximum sampling rate of 20 samples per second (for aTmega 328p at 16MHz clock)	The number of cycles in 1 sec is 50 cycles. Sampling is done every alternate cycle for 40 cycle. The average is computed during the remaining 10 cycles. Average of 10 samples gives the required frequency.
Temperature	Sampling at the rate of 12 samples per minute at 5 sec interval	

* The parameters set are temperature and the decision parameters.

5. Task Priorites

Priority 1 :- Control of power flow with system frequency.

The power flow to the heater element is proportional to the square of duty cycle. The duty cycle is dependent on frequency of the supply, as frequency is affected by loss of generation or load in the national electricity supply system. A linear profile of the duty cycle with respect to frequency has been determined, which is given below.

The response curve of duty cycle with respect to system frequency is shown in Figure 3.2. The parameters that set the slope can be input into the microcontroller and are:

(a) F1 - Lower frequency limit.

(b) F2 - Intermediate frequency limit.

(c) F3 - Upper frequency limit.

(d) DCF - Duty cycle corresponding to intermediate frequency limit.

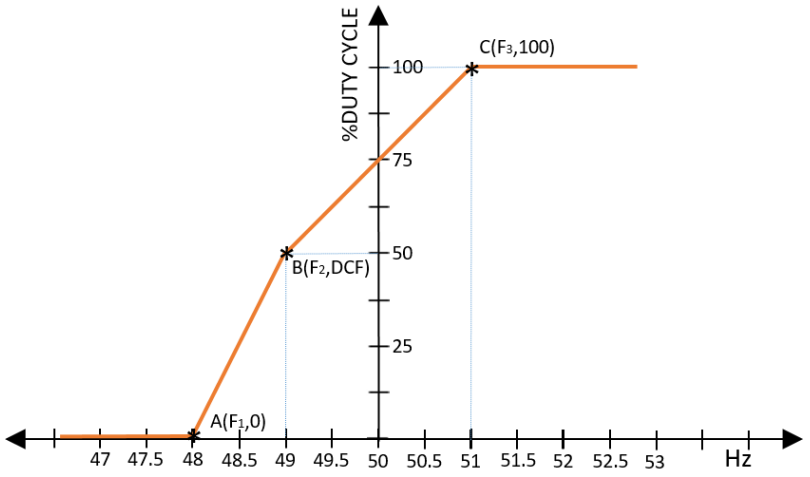


FIGURE 3.2: Plot describing duty cycle with respect to measured frequency.

Priority 2 :- Control of power flow with system voltage.

Since voltage is also a parameter which determines the state of the grid, duty cycle can also be dependent on the voltage of the grid. Figure 3.3 shows the response curve of duty cycle with respect to voltage. The parameters that are given as input to the microcontroller which help in setting the slope of the curve are:

(a) V1 - Lower Voltage limit.

(b) V2 - Upper Voltage limit.

(c) DCV - Duty cycle corresponding to lower voltage limit. 25% duty cycle is the minimum that can be defined in order to maintain continuous rectifier conduction which minimises AC system harmonics.

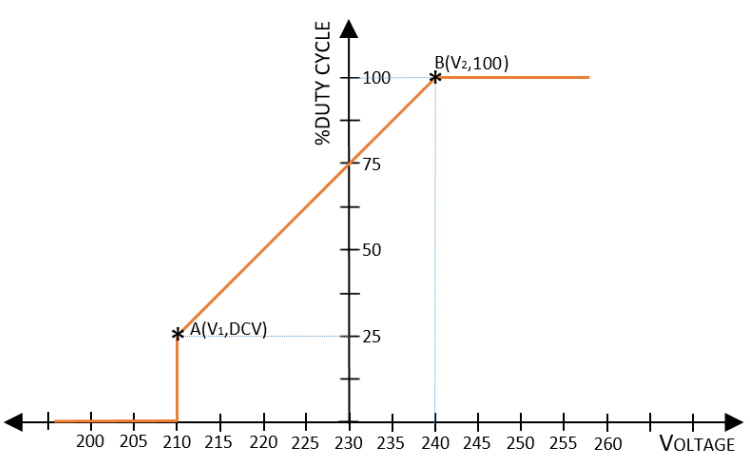


FIGURE 3.3: Plot describing duty cycle with respect to measured voltage.

Detailed determnation of duty cycle with respect to the various measured parameters is discussed in Chapter 5.

Chapter 4

Power Electronic Topology

4.1 Overview

After considering the power system operation and the need for demand side management, system requirements were specified in Chapter 3. In this chapter we discuss the various suitable power converters and compare different topologies. Simulations of three different models were developed. Switching selection and the characteristics of different models are discussed later in this chapter. The basic requirements are that the processor input is single phase mains supply and the output must be reversed at 50Hz to enable the water heating element thermal safety cut out to operate satisfactorily.

4.2 Topology Selection

Power electronic converter can be classified into many types based on their purpose, complexity and method of operation[24]. Basically power electronic converters can be classified as

1. **Power converter** :- Every power electronic circuit consists of basic conversion blocks which operate by the electronic signal generated by some control circuit. Some basic power converters are AC-DC, DC-DC, DC-AC and AC-AC converters.

2. **Power processor** :- These are power electronic circuits with many power conversion stages. The circuits use capacitors or inductors as decoupling between different operating stages.

3. **Matrix converter** :- In a power processor, the power conversion stages and the energy storage elements theoretically can be replaced by a matrix converter. In other words, matrix converters are AC-AC power converters which can be directly connected to grid without any passive elements[25]. The uniqueness of matrix converter is that the switches used in these are bidirectional. Figure 4.1 shows a typical matrix converter.

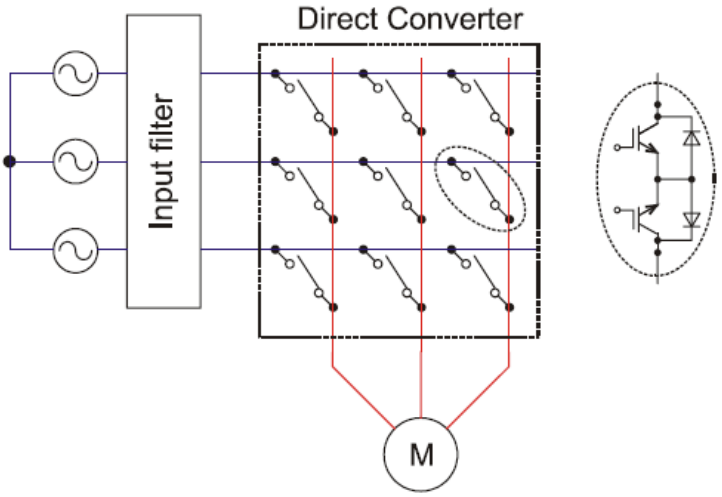


FIGURE 4.1: Basic representation of matrix inverter[26].

The proposed SDWHC involves two power conversion stages; a rectification stage which is connected to the grid and an inverter stage connected to the heater element. With power convertor technology so advanced there is a wide range of topologies and methods of designing a power converter. The following topologies were initially considered for the inverter:

1. **Single phase half bridge inverter** :- The half bridge configuration of a single phase inverter is shown in Figure 4.2. Fully controlled switches are used, for example BJT, MOSFET and IGBT . Diodes are required for free wheeling in case of inductive loads, which are usually present as body diodes in power MOSFETs and IGBTs. Here only half the rail voltage appears across the load when each switch is ON.

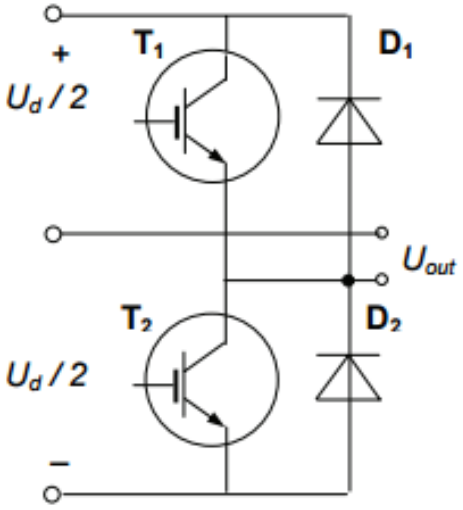


FIGURE 4.2: Single phase half bridge inverter[27].

2. **Single phase full bridge inverter** :- Two half bridges in parallel with the load connected between the two legs make a single phase full-bridge inverter, as shown in Figure 4.3. The four switches have diodes connected anti parallel (freewheeling diode) which form a path for reverse current.

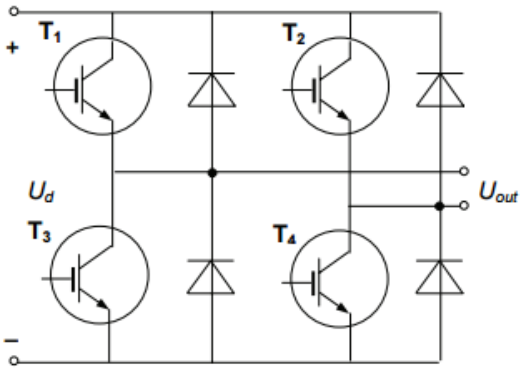


FIGURE 4.3: Single phase full bridge inverter[27].

3. **Three phase bridge inverter** :- These type of inverters are employed where the power rating is very high and the loads are three phase loads. It is similar to half bridge inverter but with three legs. Figure 4.4 shows a typical three phase inverter configuration.

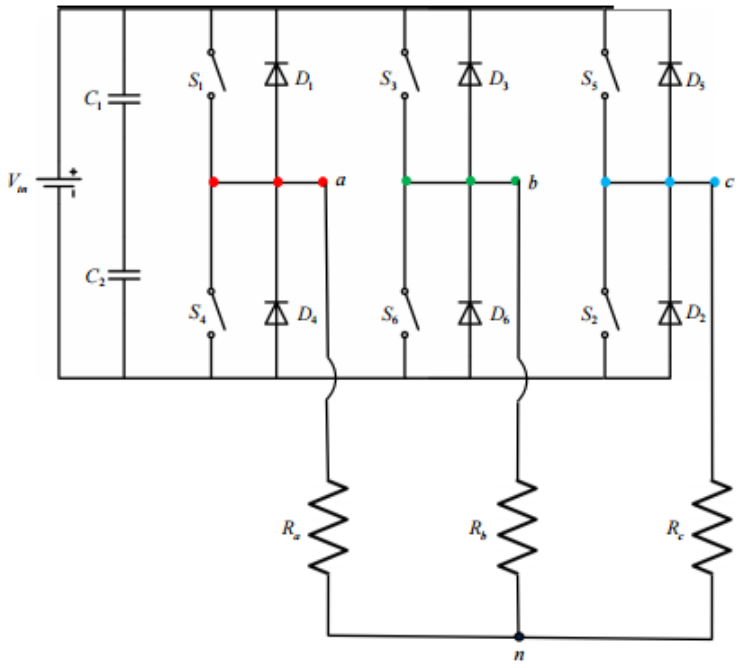


FIGURE 4.4: Three phase full bridge inverter[28].

The heater element in domestic water heater is single phase, ruling out three phase inverters or matrix inverters. Since the standards specify that only symmetric converters

can be used and half wave rectification is not allowed on AC side, a full-bridge rectifier-inverter topology is used. The next step was to determine whether an isolation was required. Two configurations of full-bridge were again considered as mentioned below:

1. Single phase full bridge with isolation (isolated system).
2. Single phase full bridge without isolation (Non isolated system).

4.2.1 Isolated Systems

Isolated inverter systems can be achieved basically in three technologies[29] as follows:

1. Isolation with 50Hz transformer :- In this technology the switches in Figure 4.5 are switched at a fundamental frequency of 50Hz and a 50Hz transformer is used as isolation. This technology is highly reliable due to its simplicity and few components, but lags behind due to low efficiency, large weight and volume due to 50Hz transformer.

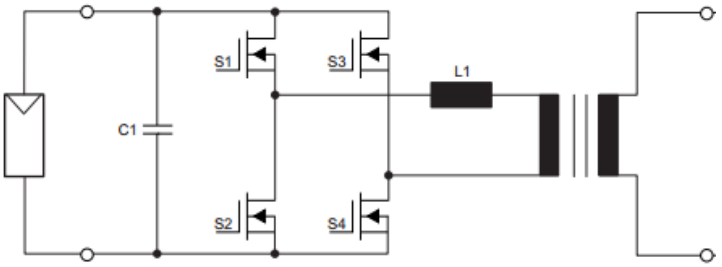


FIGURE 4.5: Isolation with 50Hz transformer[29].

2. Isolation without transformer :- Figure 4.6 shows a transformer-less technology with L1 and L2 as chokes. In this case also switches switch at 50Hz fundamental frequency. Due to the absence of a transformer, this system is highly efficient. The disadvantage is that it requires additional safety measures and requires bulky inductors.

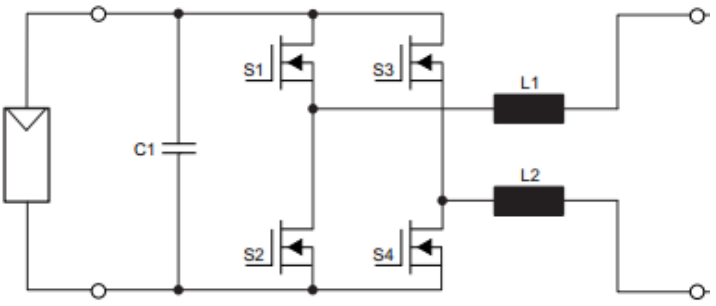


FIGURE 4.6: Isolation without transformer[29].

3. Isolation with high frequency (HF) transformer :- This technology involves multiple inverter stages. In Figure 4.7, high frequency switching (40-50kHz) is done by switches S1, S2, S3 and S4. This helps to reduce the size of transformer Tr1, whose output is again converted to DC by diodes D1 to D4. Switches S5 to S8 convert the DC to the required AC frequency. This system is compact due to the HF transformer. High efficiency is achieved by reducing transformer loss and safety is maintained by transformer isolation.

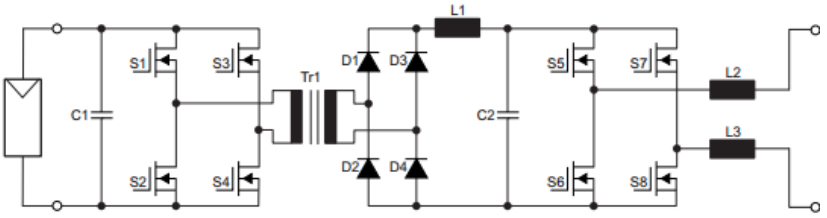


FIGURE 4.7: Isolation with HF transformer[29].

4.2.2 Non-Isolated System

Unlike an isolated system, a non-isolated system doesn't have any transformer coupling or isolation between the power converter stages. These types of converters are simple and are very compact compared to isolated counterparts. The main disadvantage is the lack of isolation makes it a risk in case of faults. The equipment without isolation should be properly earthed and should be connected to the supply mains through a MCB switch only, so that the equipment is cut-off from the mains during any fault. Figure 4.3 shows a typical inverter without isolation.

The application under consideration is essentially an AC-AC converter. An economical way to achieve this is to let the DC bus have high levels of low frequency ripple. This allows the use of a simple diode bridge rectification on the grid side and H-bridge inverter connected to heater element. It also reduces the complexity of the power converter. Since the input & output voltages are maintained and only the power flow is regulated, a single stage power converter is preferred over complex multistage power converters. The cost of controller is further reduced by using the LC filter just for removing the switching harmonics which is discussed in Chapter 5.

Next, the system was modelled in Simulink and tested. The details of testing and switching strategy selection are discussed in Section 4.3

4.3 Model Simulation and Switching Selection

Once the different topologies were studied, different switching strategies were tested by simulation. The simulations show that all the switching strategies cannot be used in an isolated model as the isolation transformer would get saturated. In an isolated model each positive cycle should be followed by a negative cycle so that transformer does not get saturated. The different topologies and switching sequences are given below.

1. **Isolated with Non-PWM switching** :- Figure 4.8 shows an isolated converter design. The isolation transformer is a HF transformer, Isolation is used in HF inverting stage, so that transformer size can be reduced.

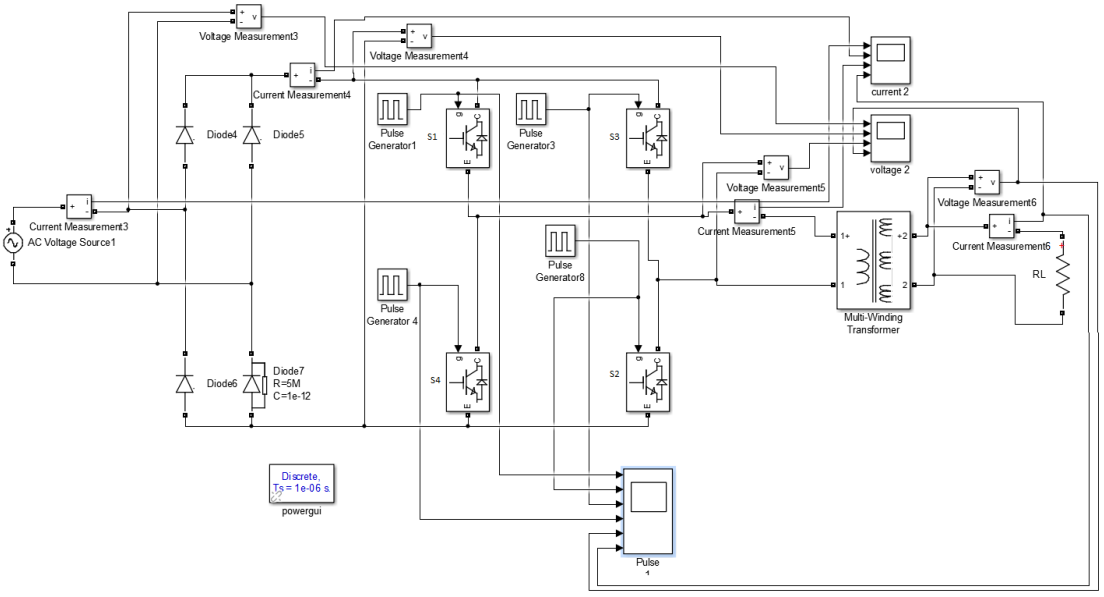


FIGURE 4.8: Simulation model with isolation.

The switching sequence employed here is such that the gate signal to S1, S2, S3 and S4 are out of phase by 0°, 90°, 180° and 270° respectively. The conduction pattern is such that when S1 and S2 are ON, a positive voltage appears across the load. A negative voltage appears across the load when S3 and S4 are turned ON. The voltage will be zero when S2 & S4 and S1 & S3 are ON. The switching pattern and waveform across the load are shown in Figure 4.9.

It can be clearly seen in Figure 4.9 (switching is done at a lower rate in order to study the waveforms) that each positive cycle is followed by a negative cycle. In this pattern of switching, the switching frequency will be two times the frequency of gate signal.

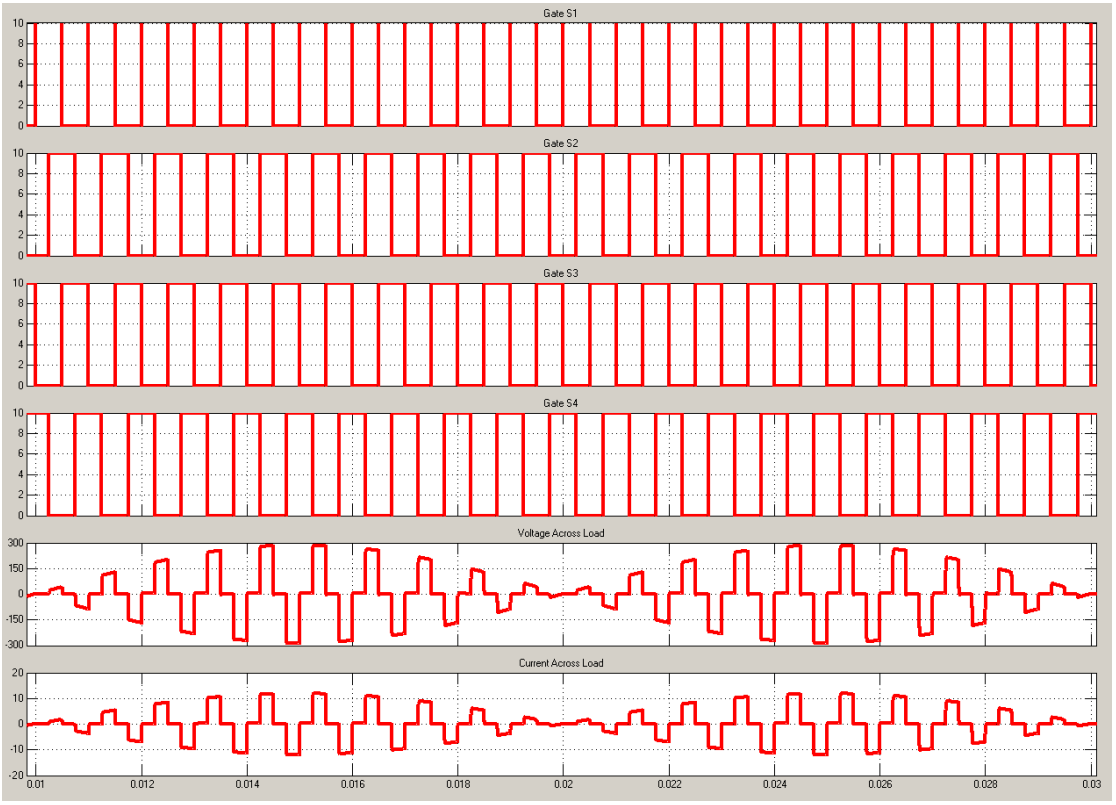


FIGURE 4.9: Waveform for model with isolation (Duty cycle of switching signal : 50% and Transformer ratio 1:1).

This model offers high safety due to the isolation, which prevents accidents due to faults. The cost is high due to the isolation transformer. The main disadvantage of this strategy is that there is no control on the voltage across the heater element. Employing a variable duty cycle switching is highly complex, high cost and lack of need for isolation rule this out.

2. **Non-isolated model with sinusoidal PWM gate control** :- An isolated model with PWM is more complex than is necessary for this application. Figure 4.10 shows the non-isolated model which was simulated. In this case the fundemental frequency of 50 Hz is maintained across the load. This is necessary for the proper functioning of the thermal cut-out switch.

   Here switches S1 and S2 conduct during one half cycle at PWM frequency, which gives a positive voltage across the load for 10ms. A negative voltage appears during the next half cycle when switches S3 and S4 conduct at PWM. The waveforms obtained are shown in Figure 4.11. Compared to the isolated circuit this model is cheaper and simpler. The control circuitry is still complex due to the PWM switching. The key advantage is that load current regularly drops to zero to allow thermal cut-out operation.

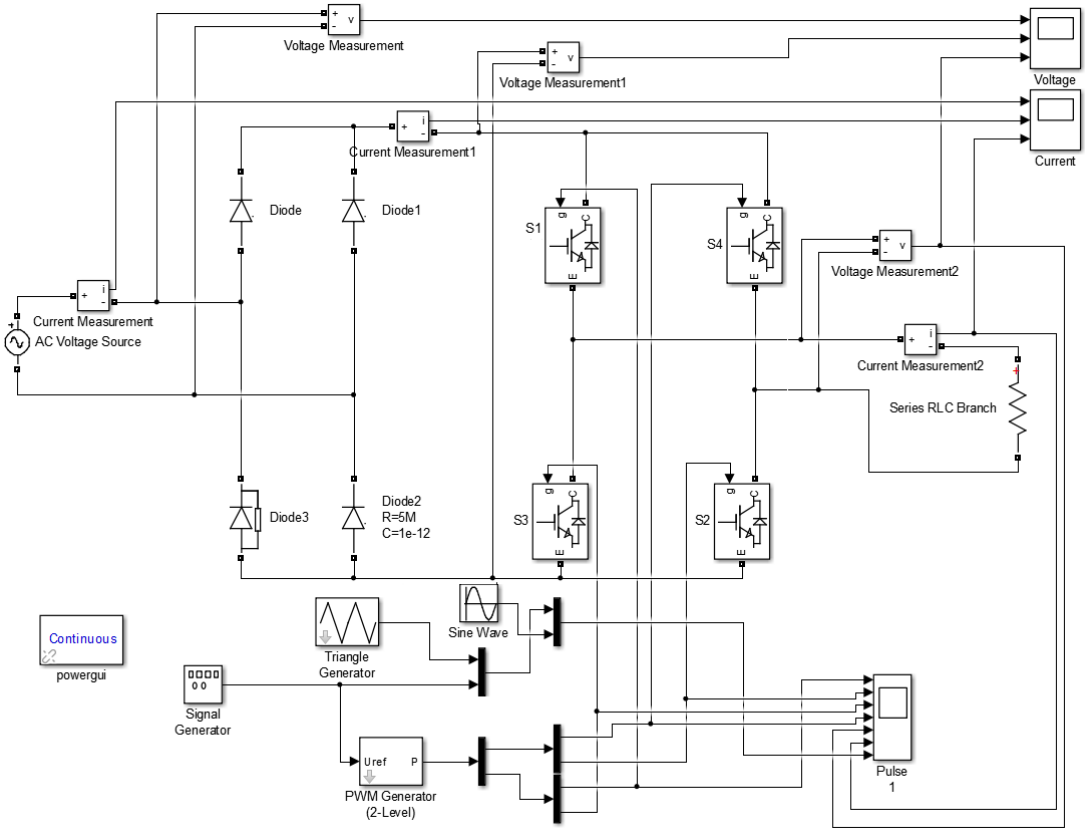


FIGURE 4.10: Non-isolated model with PWM.

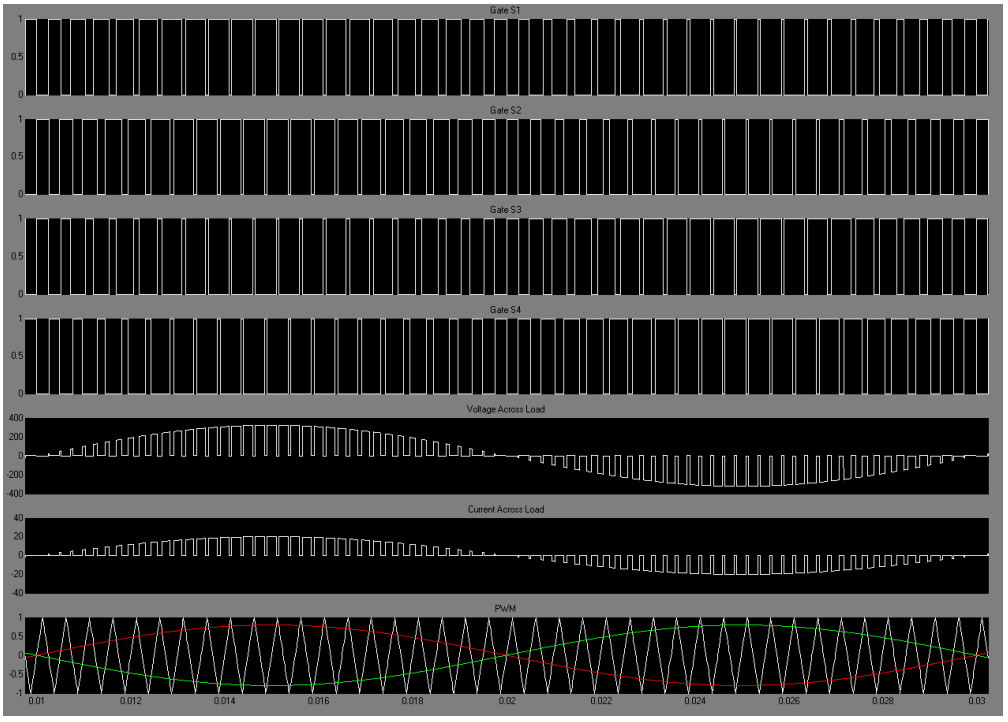


FIGURE 4.11: Switching pattern and voltage waveforms of non-isolated model with sinusoidal PWM.

Since we already have the rectified but unfiltered AC waveform on the dc bus, it is not necessary to have a sinusoidal PWM switching strategy. The circuit complexity can be reduced by using a constant duty cycle PWM.

3. **Non-isolated model with Constant PWM** :- In this application, in order to achieve an AC voltage of 50Hz across the heater element it is not necessary to use a sinusoidal PWM switching. Since, we have a DC bus which is 100% rippled bus with rectified fundamental frequency (Discussed in detail in Chapter 5) we can obtain the required AC voltage by constant PWM switching. This greatly reduces the complexity of the control algorithm. Figure 4.12 shows the simulation model.

   From Figure 4.13 it can be seen that switching is done with S2 ON and S1 switched at HF. In order to achieve a fundamental frequency of 50Hz across the load, S1 & S2 conduct during the first cycle and S3 & S4 conduct during the next cycle in a similar pattern with S3 switched at HF and S4 kept ON. Either S4 or S2 conduct during one cycle and these switch between ON and OFF state at zero crossing. The selection of frequency and determination of duty cycle is discussed in detail in Chapter 5.

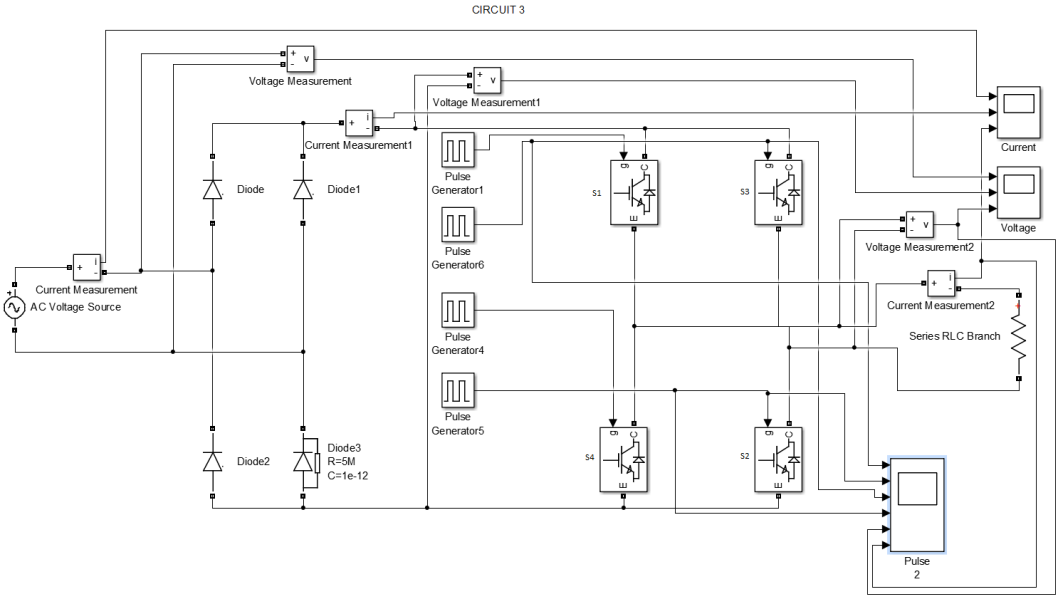


FIGURE 4.12: Simulation model of non-isolated model with constant duty cycle PWM.

After analyzing the results obtained in the above three cases along with design consideration and application purpose it was decided to use non-isolated converter with constant PWM switching. This model can be designed with least complexity and cost.

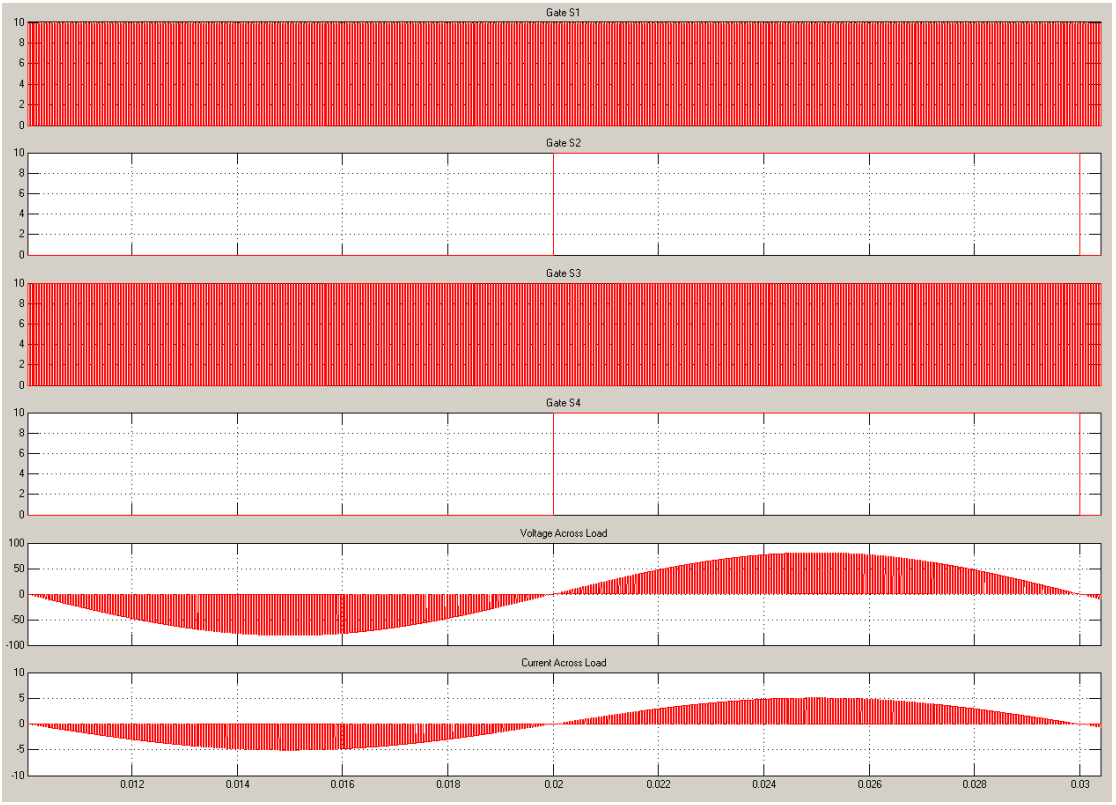


FIGURE 4.13: Switching pattern and voltage waveforms of non-isolated model with PWM.

The operating environment of a domestic water heater is well away from people, usually isolated in basements of rooms. Since they do not directly couple with the daily routines of people, a non isolated system can be safely employed.

Chapter 5

Circuit Implementation

5.1 Overview

In the previous chapters, various configurations and topologies have been discussed, and the best suited configuration was chosen. This chapter deals with the implementation of the circuit and the design steps followed. This chapter contains the following sections;

1. Power Stage
2. Gate Driver
3. Control Electronics
4. Process Controller
5. Auxiliary Supply

5.2 Hardware Design

The electronics hardware is the most important part of the Smart Domestic Water Heater controller. The major components are the power stage, control electronics/microcontroller, gate drive circuitry and control switch board power supply (SMPS) / auxiliary supply, and are identified in Figure 5.1.

5.2.1 Power Stage

This section deals with the selection of components and design of the physical configuration of the converter bridge, including selection of DC bus capacitance and switching frequency.

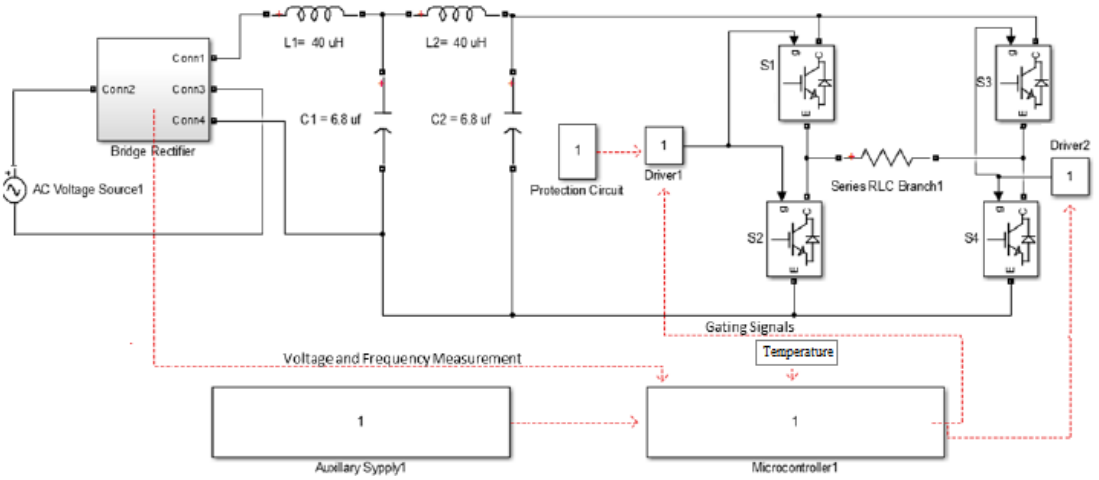


FIGURE 5.1: Hardware overview.

As in Figure 5.1 the power stage is a AC-DC-AC power converter. A bridge rectifier is used for initial conversion from ac to dc. This is a unique application when a completely rippled dc bus is used. Usually for a DC bus, it is useful to maintain a low ripple voltage. In this case the intent of the LC filter is to block the DC-AC inverter switching frequency from entering the AC supply, but to leave the characteristic rectified AC waveshape unchanged. The filter design and dc bus capacitance selection is also different which will be discussed in Section 5.2.1.5.

According to the New Zealand standards, EMI has to be maintained within limits (Refer Chapter 3 for the EMI limits). To achieve this a cascaded $(2 - stage)$ L-C filter is used. MOSFET switches in an H-Bridge configuration are used to convert from dc to ac, which is connected across the heater resistor element as in Figure 5.1.

5.2.1.1 Bridge Rectifier

The power converter is an AC-DC-AC power converter, so it is necessary to have a rectifier to convert from ac to dc. A bridge rectifier is the simplest solution. Table 5.1 shows a list of available bridge rectifiers.

Selection of bridge rectifier was straight forward. Vishay Siliconix-PB3006-E3/45 had the lowest forward voltage drop, highest voltage rating and required current rating with reasonable price. It also has a SIP case type which is easy for mounting heat sink.

This rectified voltage is stepped down using a resistor network to a low level, which is used by the control circuit for determining voltage and frequency which is discussed in Section 5.3. Refer to Appendix A for a detailed circuit diagram.

TABLE 5.1: Bridge Rectifier availability and cost comparison[30]

Manufacturer	Device	Case style	Vmax (V)	Imax (A)	Forward voltage	Price per unit (NZD)
Solid State	KBPC2504	Module	400	25	1.2	1.74
Multicomp	CM2504	GBPC	400	25	1.2	1.47
Vishay Siliconix	PB3006-E3/45	SIP	600	30	1.1	2.20
Multicomp	GBPC5006	Module	600	50	1.2	3.84

5.2.1.2 Switch Selection

This application is a high power application with moderate switching speeds and high efficiency. As shown in Figure 5.2, the MOSFET is the most appropriate device for such applications. As they are readily available and lower in cost than other options, these are the best option for this medium voltage level.

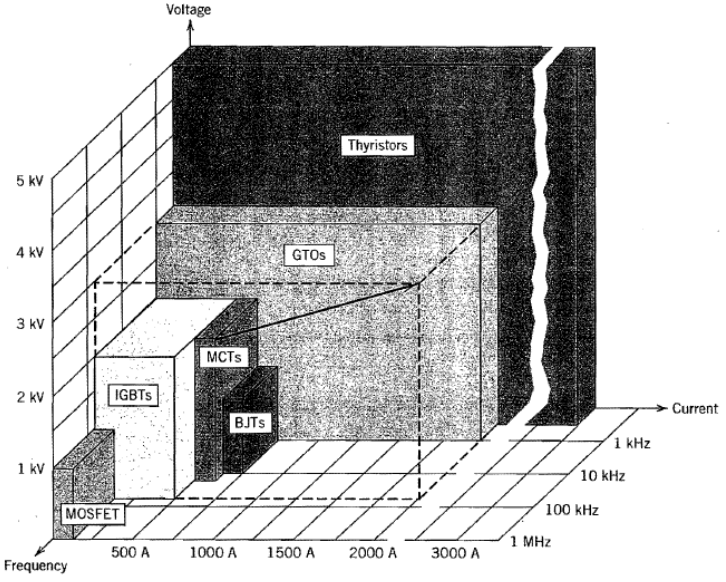


FIGURE 5.2: Various semiconductor switches available[31].

The choice of the MOSFET to be used is governed by several factors, such as electrical characteristics, form factor, device package limitations and thermal characteristics. This is explained in detail below.

5.2.1.3 Electrical Requirements

The switching devices must be capable of operating in an environment with potentials upto 350V ac. Here 400V rating is used. The other main parameter is the internal ON-resistance (R_{DSon}) which has to be low.

5.2.1.4 Package Selection

The physical device package influences the thermal characteristics and maximum current capability. For SMD devices there is a limitation to the current that can be carried by package legs and PCB pads or lands. Rather than the junction current capability, this limits the maximum current that the device can transfer in many cases. Sufficient heat cannot be radiated by small packages to ambient or a heatsink adequately even if the junctions and legs can handle the current.

The design needs to be economic, as it is a cost sensitive application. Custom heatsink extrusions, mounting plates and complicated assembly are not appropriate because of the high cost of production in small quantities. However, this application involves high current and the power dissipation is expected to be moderate. It is necessary to use a through hole device that allows for connection of an external heatsink. This would require a significant form factor change than using SMD compenents, but allows attachment to already available external heatsink. Power dissipation and heat sink design is discussed in Chapter 6.

Table 5.2 shows the power dissipation capabilities of various MOSFET packages used by Vishay Siliconix.

TABLE 5.2: Electrical and thermal parameters of various through hole packages[32].

Package	Maximum Depth (mm)	Maximum Current (A)	Maximum Temperature (°C)	Rth J-C (°C/W)
TO-247AD	5.1	73	150	0.24
Super 247	5.3	47	150	0.23
TO-247AC	5.31	70	150	0.3
TO-220 Full PAK	4.83	37	150	3
TO-220	4.65	90	175	0.6
I2PAK ($TO-262$)	4.83	50	150	0.8
HVMDIP	3.37 ($bodyheight$)	2.4	150	120
IPAK ($TO-251$)	2.39	14	150	1.1

To search for a suitable MOSFET, the major suppliers like Farnell and Digikey were consulted. Table 5.3 shows the devices in active production and readily available. Note the prices are for unit quantity.

TABLE 5.3: MOSFET availability and cost comparison

Manufacturer	Device	Vmax (V)	Imax (A)	Price per unit (NZD)
Vishay Siliconix	SIHG22N50D-GE3	500	22	5.67
STMicroelectronics	STP28NM50N	500	21	8.24
Infineon	SPW52N50C3	500	52	16.8
Vishay Siliconix	SIHG25N40D-GE3	400	25	5.49
Fairchild Semiconductor	FDP26N40	400	26	4.26
Fairchild Semiconductor	FDA24N40F	400	23	4.81

From the information provided in the device datasheet by the respective manufacturers, their electrical parameters are listed in table 5.4.

TABLE 5.4: Electrical and thermal parameters

Device	Rds Ω	Max Power Dissipation (W)	Vgs (V)	Package
SIHG22N50D-GE3	0.185	312	3	TO-247AC
STP28NM50N	0.135	150	3	TO-220
SPW52N50C3	0.06	417	3	TO-247
SIHG25N40D-GE3	0.14	278	3	TO-247AC
FDP26N40	0.13	265	3	TO-220
FDA24N40F	0.15	235	3	TO-3PN

After considering the power dissipation and heat sink requirement, which will be discussed in Chapter 6, the MOSFET supplied by Fairchild Semiconductor FDP26N40 found to meet the requirement. Even though Infineon - SPW52N50C3 has lower turn on resistance and highest power dissipation, the high value of reverse transfer capacitance causes longer switching transitions and thereby high power dissipation during switching.

5.2.1.5 Filter Design

A filter is necessary to regulate the harmonics within standard limits. As discussed in Section 5.2.1 a cascaded L-C filter is used. Since the PWM switching frequency is 31kHz as provided from the microcontroller, and after simulating various designs in Matlab, the filter has been designed at a cut-off frequency of 10kHz.

The cut-off frequency of a single stage LC filter occurs when

$$X_L = X_C, \tag{5.1}$$

or

$$\omega L = \frac{1}{\omega C} \tag{5.2}$$

Solving for ω,

$$\omega = \omega_0 \quad = \frac{1}{2\pi\sqrt{LC}} \tag{5.3}$$

$$f_0 = \frac{\omega_0}{2\pi} \quad = \frac{1}{2\pi\sqrt{LC}} \tag{5.4}$$

Where	X_L	Inductive reactance.
	X_C	Capacitive reactance
	ω	Frequency in radians.
	ω_0	Cut-off frequency in radians.
	L	Inductance (H)
	C	Capacitance (F)
	f_0	Cut-off frequency in Hz

Since readily available inductor values are limited, a 40μH 26A inductor available from Farnel was chosen, refer to Appendix C for device specification.

The capacitor value is determined from equation 5.4 with inductor value as 40μH and cut off frequency of 10kHz. The calculated capacitor value was 6.33μF. The nearest available capacitor is 6.8μF. A 6.8μF 630V DC metal film capacitor with 20% tolerance was used. The prototype was implemented and tested with the above filter as detailed in Chapter 7.

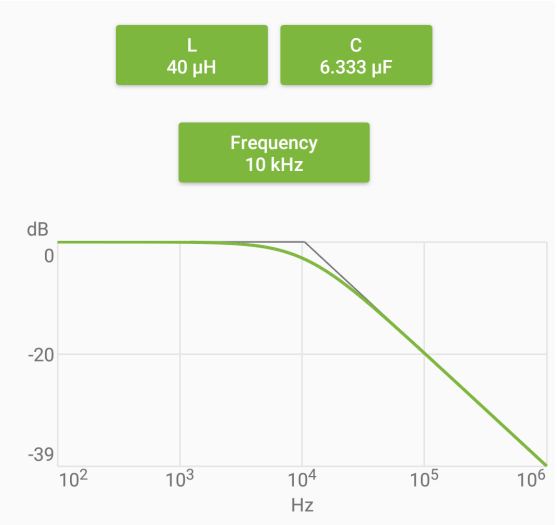


FIGURE 5.3: Frequency response of single stage L-C filter.

The filter circuit operates well at duty cycle greater than 50%. It limits the switching frequency harmonic currents in the ac supply to acceptable levels, and leaves the characteristic rectified AC waveform on the dc bus unaffected.

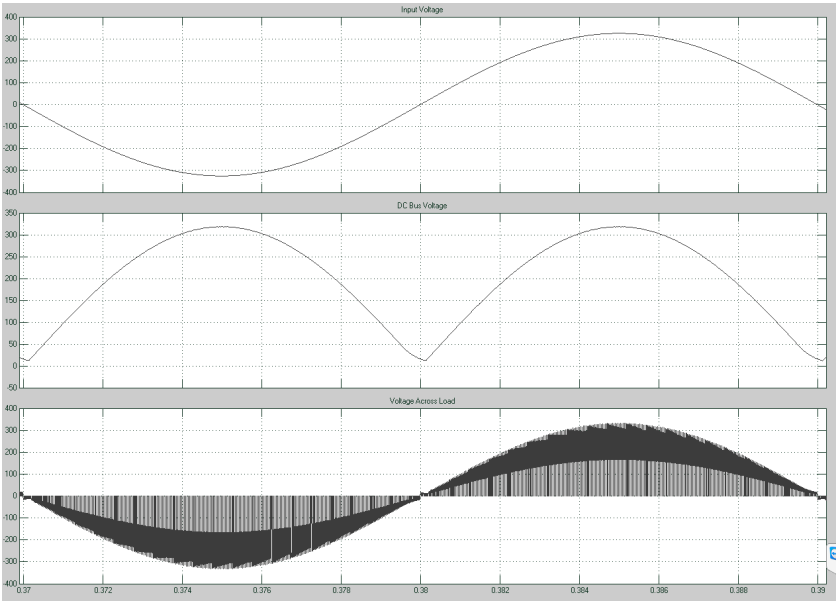


FIGURE 5.4: Simulation result of the converter with 2-stage filter.

Test Condition :	Switching frequency	31kHz.
	Capacitance	6.8 μF
	Inductance	40mH
	Duty cycle	50%.

However, at lower duty cycle, the two capacitors are not discharged sufficiently quickly by the load to leave the characteristic dc bus ripple unaffected. This in turn affect the water heater element thermostat operation as well as the AC side harmonics.

This is shown in Figure 5.5, which shows the same circuit in operation with a 25% duty cycle.

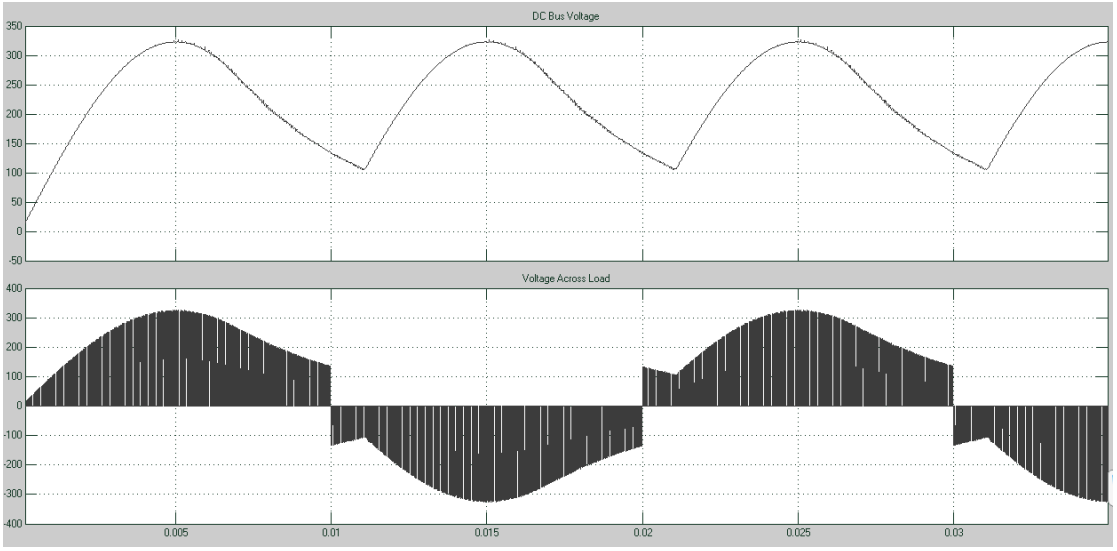


FIGURE 5.5: Simulation result showing distortion of DC Bus due to discontinuous rectifier conduction.

This can be solved in two ways - firstly, by limiting the duty cycle to be greater than the minimum value or secondly, by modifying the filter to have larger inductance with smaller capacitance.

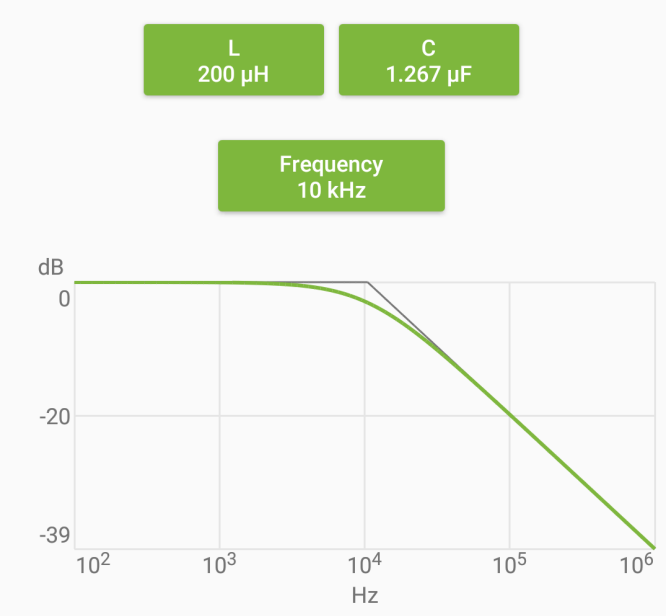


FIGURE 5.6: Frequency response of revised L-C filter.

The simulation was again conducted with a 1.2μF capacitor and 200mH inductor. DC bus waveforms were studied with various duty cycles. After mutiple iterations with duty cycle, the results suggested that with above mentioned L and C values the possible range of duty cycle was determined to be between 25% and 95%. The results obtained during simulation is shown in Figure 5.7.

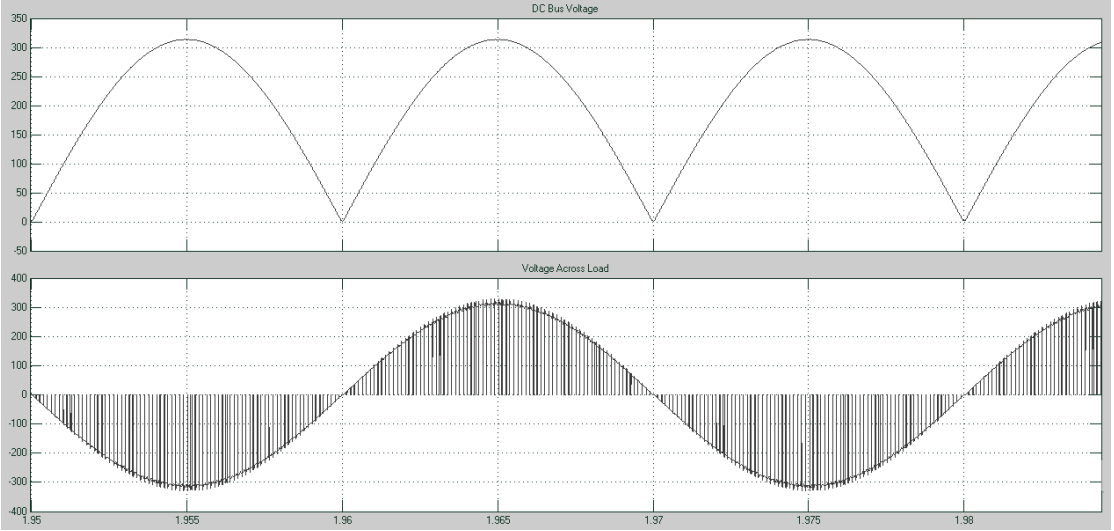


FIGURE 5.7: Simulation result with revised L-C value and at 25% duty cycle.

The duty cycle had to be limited at 95% due to limitation of the gate drive, which will be discussed in Table 5.5.

This is a design limitation, as capacitor size was reduced, inductor size increases. This in turn increases the cost, as larger inductors are more expensive.The above factors put a constraint on the variation of duty cycle. The prototype was tested with initial filter design, after testing the filter design was reconsidered. Detailed harmonic analysis of the system with revised LC values is discussed in Chapter 7.

5.2.2 Gate Driver Design

In a power converter the switches are often connected to high rail voltages. In order to turn on a switch a voltage has to be applied to the gate of the switch, generally varying from 5V in low power applications upto 25V in high power applications. The control circuitry or the processor are low power circuits with maximum voltage levels of 5 volts and few milli amperes. A gate driver is required to interface between the control circuitry and the switches.

5.2.2.1 Gate Drive Requirements

High performance gate drive circuits are required to achieve high system efficiency in high frequency switching power electronic devices. MOSFETs shoud be switched ON and OFF in the shortest possible time, a process which usually takes between 10 and 60 ns. During this transition time, current I_D begins to flow into the drain. Yet voltage V_{DS} has not reduced to its minimum level. The effective ON resistance of the device is high, resulting in the dissipation of power. At high switching frequencies, there is an increase in the power dissipation due to the increased number of switching events.

The gate drive characteristics of a MOSFET are shown in Figure 5.8. Each of the four phases can be defined as:

1. C_{GS} charges, gate voltage rises to threshold voltage
2. Linear transition region
3. Miller plateau- constant gate voltage, but V_{DS} decreases
4. Final turn on stage, gate current decreases

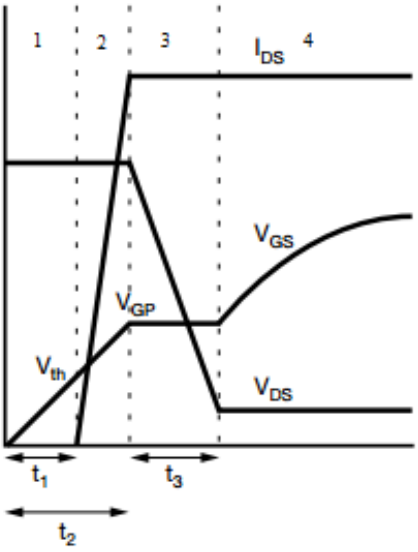


FIGURE 5.8: Turn on characteristics of MOSFET[33].

The switching circuit aims for a transition through regions 2 and 3 as quickly as possible so as to reduce the power dissipation of the device. The maximum switching speed at which this can occur is defined by the combination of the gate capacitance of the MOSFET, the driving voltage, MOSFET characteristics, internal impedance of the driver

circuit and any series resistance. The gate driver circuit should be designed to maximize current source capability as the MOSFET passes through the Miller Plateau region (stage 3).

5.2.2.2 Gate Drive Selection

Component selection and technical design need to be done carefully in the construction of such a circuit. Bootstrap drive circuits are available in integrated circuit packages, with only the bootstrap capacitor and diode required as external parts. Integrated buffering is included in these driver ICs to provide dead time between top and bottom switch conduction to reduce the possibility of shoot-through at the switching transitions. Table 5.5 shows list of gate driver options available.

For this design, a bootstrap circuit is the most appropriate method as it is cheap and a well understood option. It is the normal industry practice for this power and voltage level. A bootstrap circuit works by charging a capacitor C_{BOOT} (as in Figure 5.9) during the switch's OFF time. When the switch is turned ON, the negative end of the capacitor rises with the MOSFET source so that the voltage across C_{BOOT} is available to drive the MOSFET gate.

From a variety of half bridge ICs which are available at low cost, Fairchild Semiconductors FAN73933 Half bridge gate drive IC was chosen. A typical configuration is shown in Figure 5.9. It has very high sinking and sourcing capacity at 2.5A/2.5A, inbuilt default dead time of 200ns, 3.3V and 5V logical input levels. FAN73933 also has separate ground and common pin which isolates the control electronics from the power circuit.

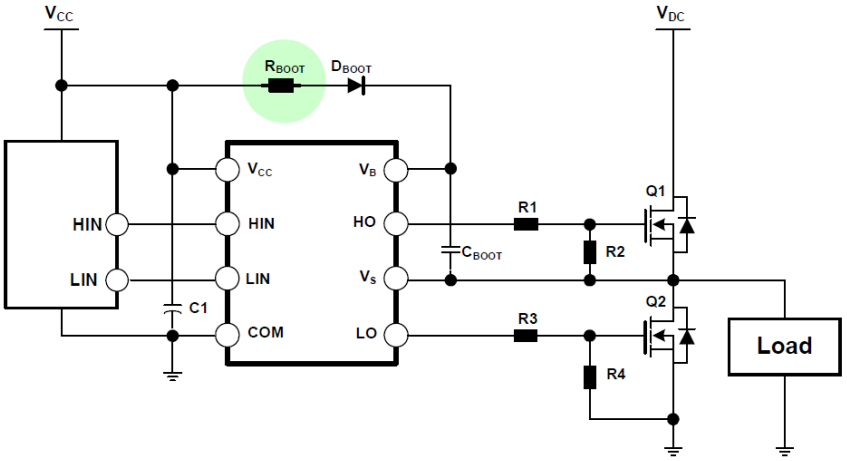
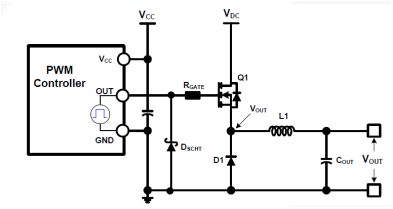
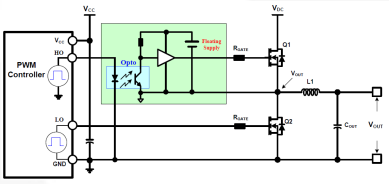
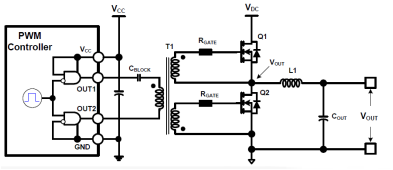
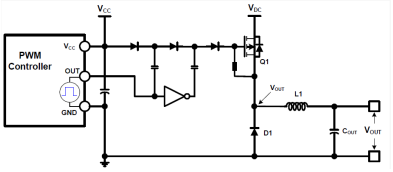
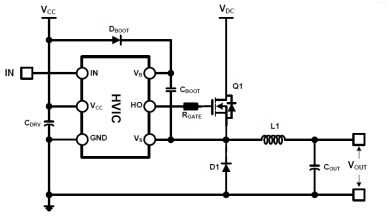


FIGURE 5.9: Typical bootstrap driver circuit[34].

TABLE 5.5: List of various gate drive circuit[34].

Method	Basic Circuit	Description
Direct Drive		Easiest high-side application, the MOSFET can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows : $V_{CC} < V_{GS,MAX}$ and $V_{DC} < V_{CC} - V_{GS,Miller}$
Floating Supply Gate Drive		Cost impact of isolated supply is significant. Optocoupler tends to be relatively expensive, limited with bandwidth and noise sensitivity.
Transformer Coupled Drive		This driver can drive gate at 100% duty cycle for an indefinite period of time, but has limited switching performance. This can be improved with adding complexity to driver design.
Charge Pump Drive		The turn-on times tend to be long for switching applications. Ineffi-ciencies in the voltage multiplication circuit may require more than low stages of pumping.
Bootstrap drive		Simple and inexpensive with limitations; the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor.

5.2.2.3 Bootstrap Components

The bootstrap capacitor is one of the key components in a bootstrap circuit. The bootstrap capacitor must provide the energy to charge and maintain the voltage on the MOSFET gate and provide the quiescent current for the gate drive IC.

With referance to application note AN-978[35] and AN-6076[36] , C_{boot} is calculated as per equation 5.5.

$$C_{BOOT} \geq 2 * \frac{Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE})t_{ON} + Q_{LS}}{V_{DD} - V_F - V_{GSMIN}} \tag{5.5}$$

Where	Q_{GATE}	Switch total gate charge
	I_{LKCAP}	Capacitor (C_{BOOT}) leakage current; 0mA for ceramic capacitor
	I_{LKGS}	Switch gate-source leakage current
	I_{QBS}	Bootstrap circuit quiescent current
	I_{LK}	Bootstrap circuit leakage current
	t_{ON}	High-side switch on time
	Q_{LS}	Charge required by the internal level shifter; 3 nC for all HIV drivers
	V_{DD}	Driver supply voltage
	V_F	Bootstrap diode forward drop
	V_{GSMIN}	Minimum gate-source voltage.

It can be seen from Figure 5.9 that as the negative end of the bootstrap capacitor floats with the bridge mid-point, it is exposed only to V_{DD} and not the full bridge voltage. A minimum capacitor value of 238nF is obtained by evaluating Equation 5.5 for this application. The application note suggests a rule that this capacitor should be connected to a decoupling capacitor whose value should be 10 times C_{BOOT} to ensure there is sufficient capacitance, i.e. approximately 2.3μF. This is within the range available from surface mount multilayer ceramic capacitors in an 0805 package, such as the MuRata Hi-Cap range. Since 238nf and 2.3μ F is not available 220nf and 2.2μ F capacitor are used as C_{BOOT} and decoupling capacitor respectively.

The selection of the bootstrap diode should be done in such a way that it can block the full power rail voltage (in this case 400 V max) and should be capable of supplying a maximum current of not less than the charge on the bootstrap capacitor times the frequency of operation. It should also be a fast recovery device in order to minimize the current fed back into the Vcc supply. Details of selected components is given in Appendix A.

5.2.2.4 Gate Resistance

In order to reduce the transition time and power dissipation during switching, it would be desirable to minimize the series resistance between the driver and the MOSFET (as in Figure 5.9) and therefore maximize current. However this is not always appropriate. The parasitic inductance in the PCB tracks between the driver and MOSFET device can resonate with the input capacitance of the switching device. This high Q resonant circuit can be excited by the step edges of the gate drive waveform. Hence oscillatory spikes are observed in most gate drive circuits.

By appropriately choosing R_G, the total resistance between the driver and the MOSFET gate, the oscillations and overshoot in the gate drive can be minimised.

With reference to application note AN-7003[37] and AN-6076[34] , R_g is calculated according to the equation 5.8

$$I_{g(avg)} = \frac{Q_{gs} + Q_{gd}}{t_{sw}} \tag{5.6}$$

$$R_{Total} = \frac{V_{DD} - V_{gd(th)}}{I_{g(avg)}} \tag{5.7}$$

$$R_{DRV(ON)} = \frac{V_{DD}}{I_{SOURCE}} \tag{5.8}$$

$$R_{GATE} = R_{Total} - R_{DRV(ON)} \tag{5.9}$$

Where	$I_{g(avg)}$	Average gating current required.
	Q_{gs}	Gate to source gate charge
	$V_{gd(th)}$	Gate to drain Miller charge.
	t_{sw}	Switching time
	R_{Total}	Total resistance in entire gate drive path
	$R_{DRV(ON)}$	Driver equivalent on resistance
	R_{GATE}	Gate resistance (R1 and R2 in Figure 5.9)

From equation 5.6, 5.7, 5.8 and 5.9 along with data from device datasheets R_{GATE} is calculated as 15Ω. The gate resistor must meet certain performance requirements and have certain features in order to be able to withstand the substantial load that occurs in application. The following are the main features required for a gate resistor:

1. Surge proof.
2. Metal film.
3. Low temperature coefficent, Tight tolerances.

Metal film resistors are suitable due to their low inductance.

5.3 Control Electronics

5.3.1 Voltage Measurement

Voltage is one of the main parameters to be monitored for the present application. There are many techniques for determining the r.m.s value of voltage, which are by using:

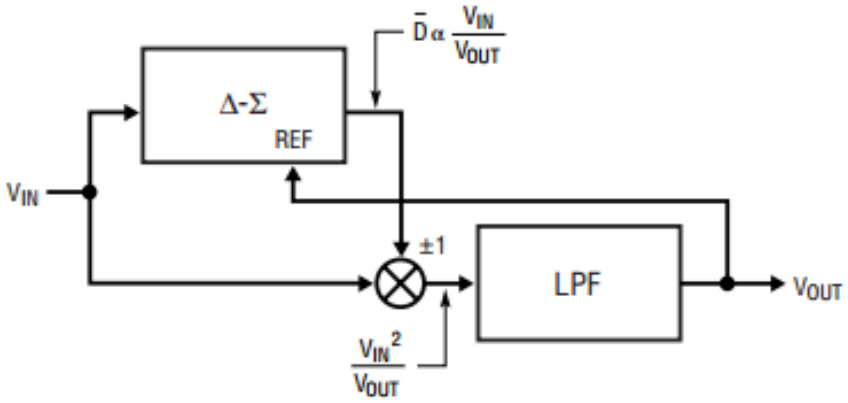
1. DSP Programming.
2. Analog measurement IC's.

In this case, since a low computation micro controller is being used as discussed in Section 5.4, an analog IC is used. An Integrated Circuit LM 17996 RMS to DC converter is used. Specifications of the IC are as follows.

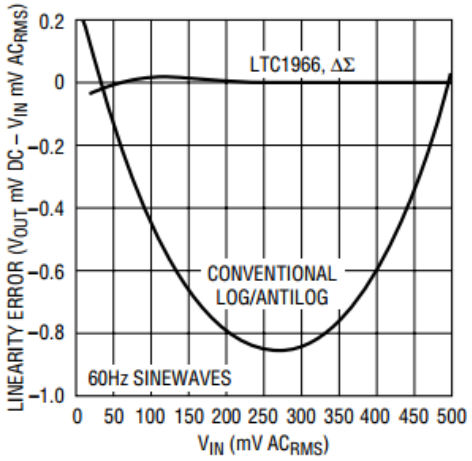
TABLE 5.6: Specification for LTC 1966 from datasheet

Feature	Description
Accuracy	0.1% Gain Accuracy from 50Hz to 1kHz 0.25% Total Error from 50Hz to 1kHz
Linearity	0.02% Linearity Allows Simple System Calibration
Supply Current	.155mA Typ, .170mA Max
Flexible Supplies	2.7V to 5.5V Single Supply Up to 5.5V Dual Supply
Flexible Inputs	Differential or Single-Ended Rail-to-Rail Common Mode Voltage Range Up to 1VPEAK Differential Voltage
Wide Temperature Range	–55° C to 125° C

LTC 1966 uses implicit computation to determine the RMS Value.



(A) Topology for LT1966



(B) Graph showing linearity and percentage error[38]

FIGURE 5.10: Parameters of LTC1966[39].

As shown in Figure 5.10A, the topology can be analyzed easily. It starts with identification of the input and output of the Low Pass Filter (LPF). The input to the LPF is obtained from the multiplier or divider in the form of

$$V_{OUT} = \frac{\overline{(V_{IN}^2)}}{V_{OUT}} \tag{5.10}$$

Here we have output as DC, therefore

$$V_{OUT} = \frac{\overline{(V_{IN}^2)}}{\overline{V_{OUT}}} \quad = \frac{\overline{(V_{IN}^2)}}{V_{OUT}} \tag{5.11}$$

Simplifying equation 5.11, we get

$$V_{OUT} = \sqrt{\overline{(V_{IN}^2)}} \quad = rms(V_{IN}) \tag{5.12}$$

As per the specifications, the differential input to LTC1966 is only $1V_P$. As discussed in Section 5.2.1.1, the voltage is stepped down using a resistor divider network. The stepdown voltage signal is fed to LTC1966 for measurement. Figure 5.11 shows the configuration connection diagram of LTC1966.

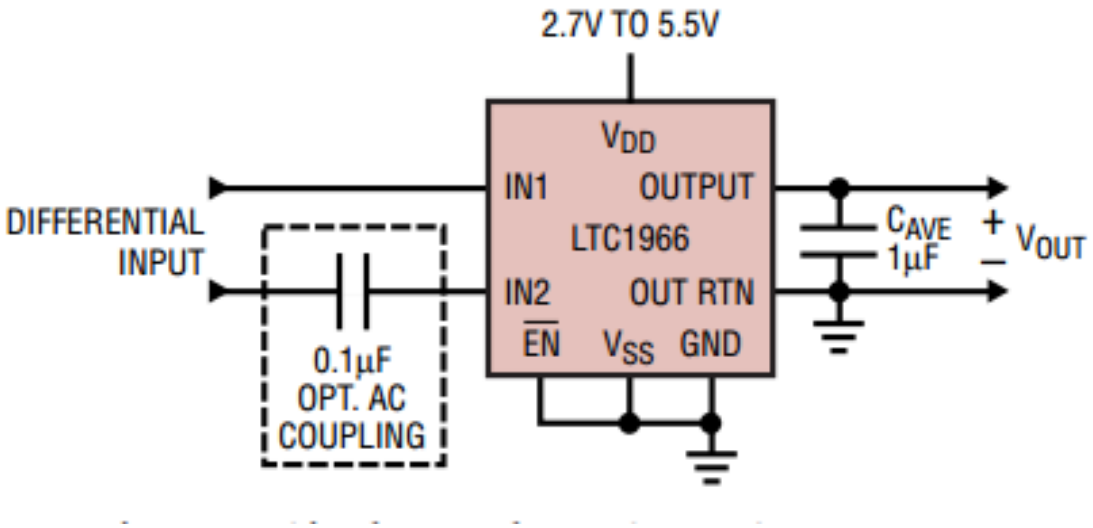


FIGURE 5.11: Connection of LTC1966[38].

The DC output is fed into the A/D converter of the microcontroller. Further measurements and calibration are done in the microcontroller, which will be discussed in detail in Section 5.4.5.

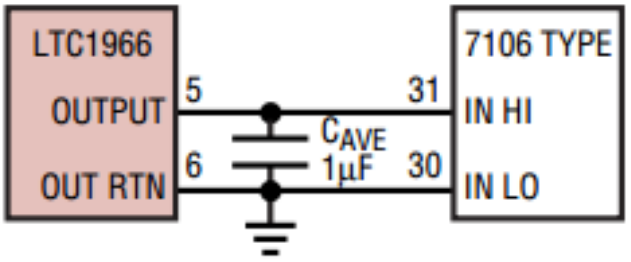


FIGURE 5.12: Interfacing for LTC1966 to ADC/Microcontroller[38].

5.3.2 Frequency Measurement

Frequency is another key parameter that has to be measured. Since frequency doesn't change immediately during a fault, there is no requirement of rapid measurement. Hence frequency measurement is done using the microcontroller. For the microcontroller to measure frequency, analog signals have to be first converted to a digital signal. An electronic circuit is used for this conversion.

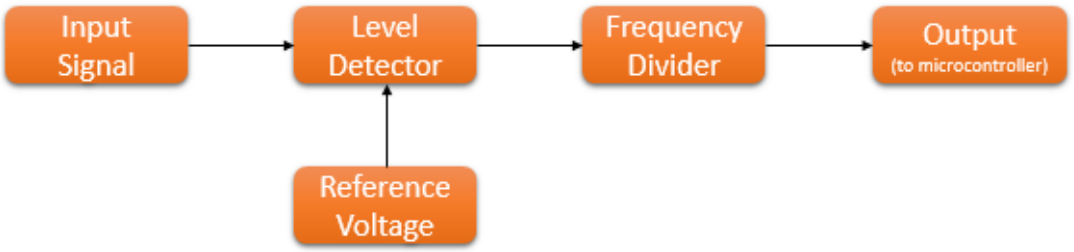


FIGURE 5.13: Block diagram of frequency measurement circuit.

The input signal here is the rectified signal obtained in Section 5.2.1.1. Since this rectified signal has twice the input frequency, direct measurement would give an incorrect frequency value. Initially, an Op-Amp comparator is used, which is set at 450 mV. The Op-Amp gives a high value when the input signal is less than 450 mV. A square pulse of the same frequency is obtained, as shown in Figure 5.15.

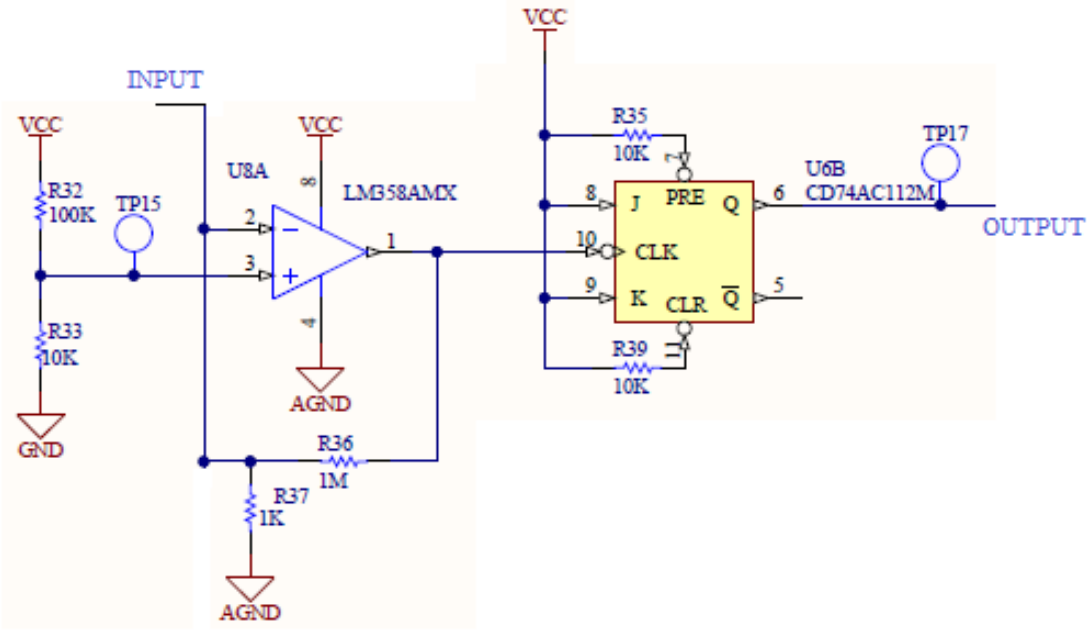


FIGURE 5.14: Implementation of frequency measurement circuit.

To reduce the frequency, a J-K flip-flop is used. The negative edge triggered J-K flip flop is used with the J and K pulled to high, and the output of the Op-Amp is fed as input to clock. This acts as a frequency divider circuit and the output of the J-K flip flop has the same frequency as that of the grid frequency. Figure 5.14 shows a detailed circuit.

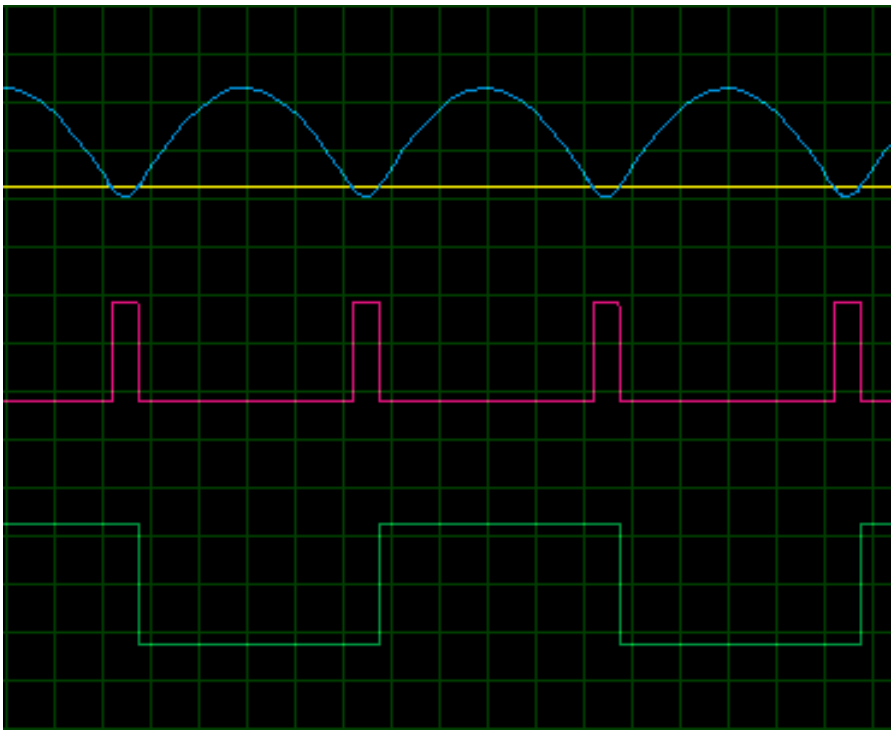


FIGURE 5.15: Wave form obtained during simulation of frequency measurement circuit in Proteus.

Figure 5.15 shows the expected plot and waveform which was simulated in Proteus, a simulation software from Labcenter Electronics. Signal 1 (yellow) gives the reference level, which is fed into the non inverting terminal of Op-Amp. Signal 2 (blue) is the input signal to the inverting terminal of which frequency is to be measured. Signal 3 (pink) is the output of the OP amp, having pulses of the same frequency as the input signal. Signal 4 (green) is the output of the J-K flip flop, and is the required signal. It is of the same frequency as that of the grid frequency, and is fed into the digital port of the microcontroller, where time period between consecutive falling edges is measured, which is discussed in detail in Section 5.4.

A secondary circuit using transistors is also employed in the circuit. This is used solely for calibration purpose as the transistor circuit has certain draw-backs.

The transistor in Figure 5.16 during turn-on, clips the wave form at 4V. This distorts the actual wave form which in turn affects the RMS voltage measurement. Due to this drawback this circuit cannot be used during actual operation of the system. A jumper

(selector) J3 is used to switch between the two circuits. For detailed circuit diagram refer appendix A. Circuit along with built-in software function in Arduino (FreqMeasure) is used to compute the frequency during calibration.

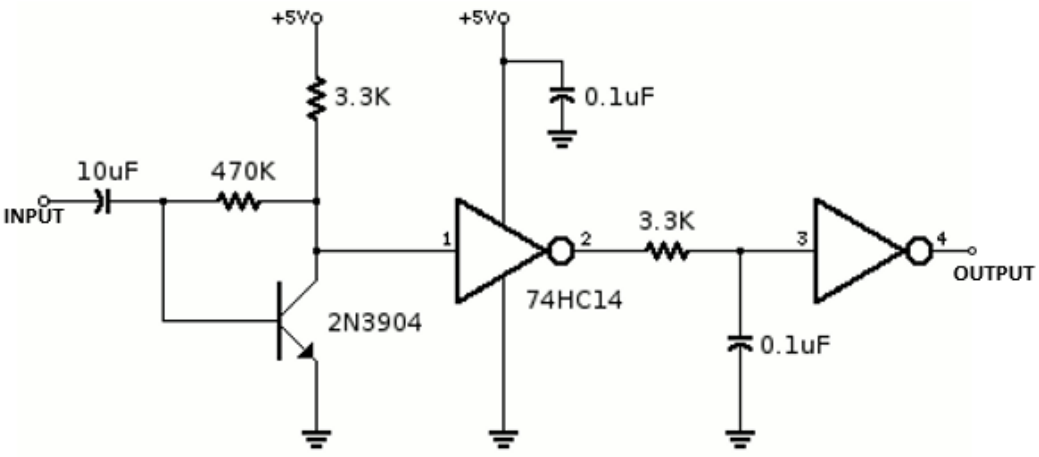


FIGURE 5.16: Secondary circuit used for measuring frequency during calibration[40].

5.3.3 50Hz Tracking Circuit

In order to meet the requirements of the thermostat and safety thermal cut-out, the supply to the water heater element should have a frequency of 50 Hz with zero crossing so that they can cut off when the temperature level of water exceeds the limits.

For achieving this, low side switches are switched at 50 Hz. To reduce switching losses, low side switches are switched at zero crossings. Since the signal fed to the control circuitry is the full wave rectified voltage obtained in Section 5.2.1.1, it is difficult to detect the zero crossing. Hence a level detection along with a timing circuit is used to serve the purpose.

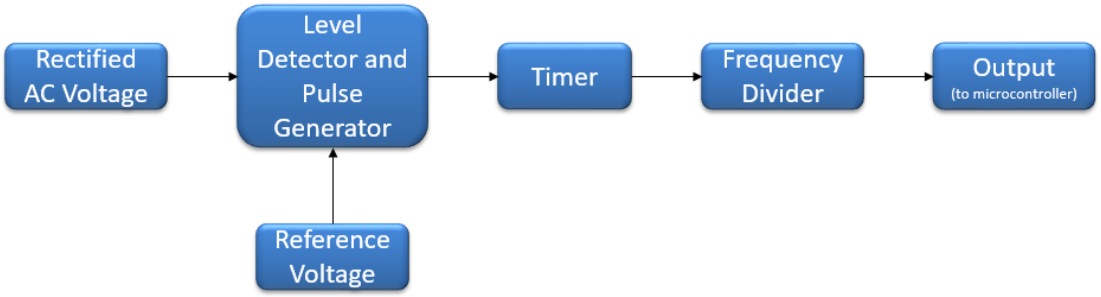
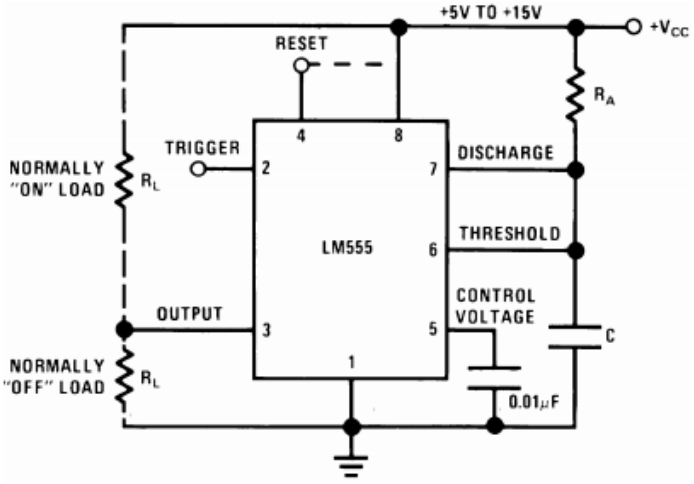


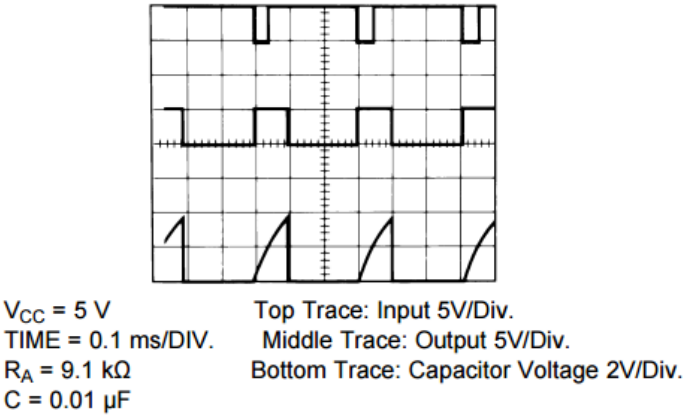
FIGURE 5.17: Block diagram for 50Hz tracking.

The time period of the signal is given by

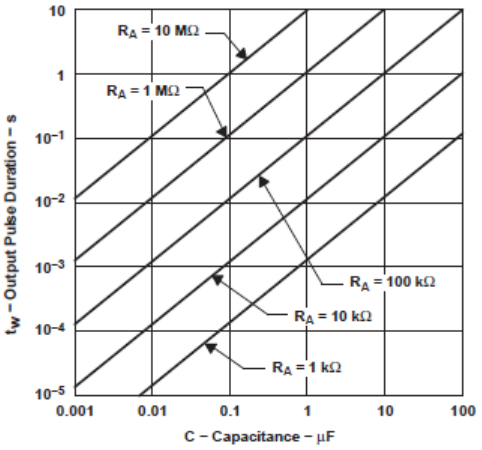
$$T = \frac{1}{Frequency} \tag{5.13}$$



(A) 555 Timer in mono-stable configuration.



(B) 555 Timer in mono-stable sample waveform.



(C) Graph showing pulsetime for various values for R and C

FIGURE 5.18: 555 Timer configuration and parameters[41].

Using equation 5.13 the time period of the rectified AC voltage is 10ms. we also assume that the voltage waveform is linear when θ is small, since the signal here is a rectified sine wave for small values of θ $\sin\theta \propto \theta$.

From the above assumption, for a 5 volt(peak) wave the time required to reach 10% of its voltage will be 10% of the time period T. Therefore time to reach .5V is 1ms

An Op-Amp comparator is employed with the level set as .5V (practically .459 V). The pulse generated acts as a trigger for the timer circuit. The falling edge of the pulse marks 10% of the time period. The timer circuit is designed so that the falling edge of the timer will be at zero crossing.

The timer circuit is a 555 timer in mono-stable mode as shown in Figure 5.18A used with ON time at 90% of the time period, i.e. 90% of 10 ms = 9 ms, with the falling edge of level detection as trigger.

The R and C values as in Figure 5.18A are calculated according to the equation 5.14

$$t_{on} = 1.1RC \tag{5.14}$$

Even though the output of the timer circuit has a falling edge at zero crossing, the frequency continues to be 100 Hz. In order to reduce the frequency, a J-K flip flop is used again in toggle mode, with the output of 555 timer as clock signal. It is then given to some logic circuitry, which will be discussed in Section 5.3.5.

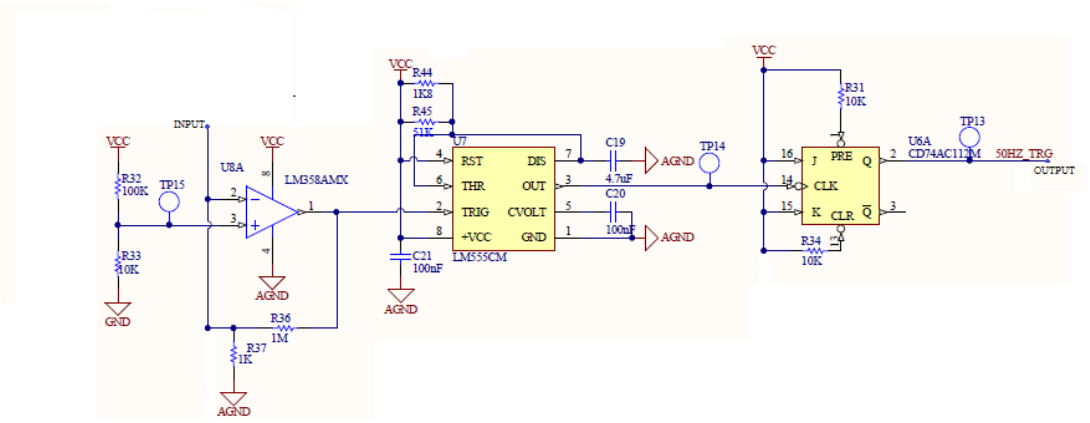


FIGURE 5.19: Implemented circuit for 50Hz tracking.

With respect to Figure 5.20, channel 1 shows the rectified input signal which is given to the level detector. Channel 2 is the output from the level detector, with the output high when the input is less than 0.459 V. The output of the level detector will have a falling edge at 1 ms (10% of the time period). Channel 3 is the output of the timer

with ON time 9ms (8.97 ms). The small change is due to the tolerance of resistors and capacitors. The output of the J-K flip flop with the required frequency of 50 Hz is obtained in channel 4.

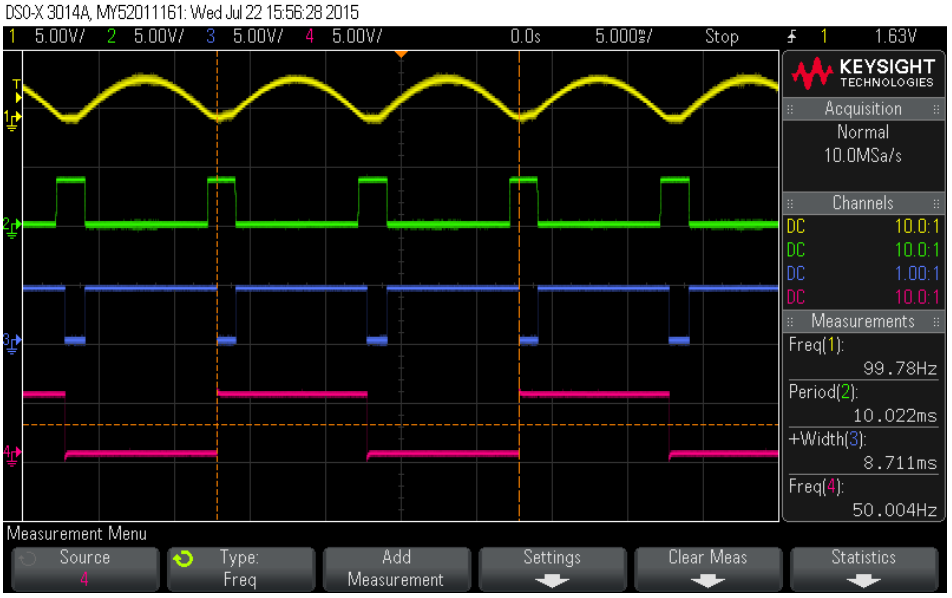


FIGURE 5.20: Waveforms obtained from frequency tracking circuit.

5.3.4 Shoot Through Protection

Even though the two half bridge gate drivers are used with built in dead time, there is a possibility that a shoot through can occur. Hence a shoot through detection circuit is employed. The circuit is designed in such a way that when shoot through protection is active, the signal to gate driver does not pass the gate control circuit, which is discussed in detail in Section 5.3.5.

A current measurement circuit consisting of a resistor and an Op-Amp is used to detect the potential across the resistor, as shown in Figure 5.21. The Op-Amp is used as a comparator.

The reference voltage can be set according to the shoot-through current value, and is provided to the inverting terminal of the Op-Amp. The non-inverting terminal is connected to one end of the resistor as shown in Figure 5.21. For prototype testing the cut-off current is set at 16A. The reference voltage is set at 0.16V using a voltage divider circuit.

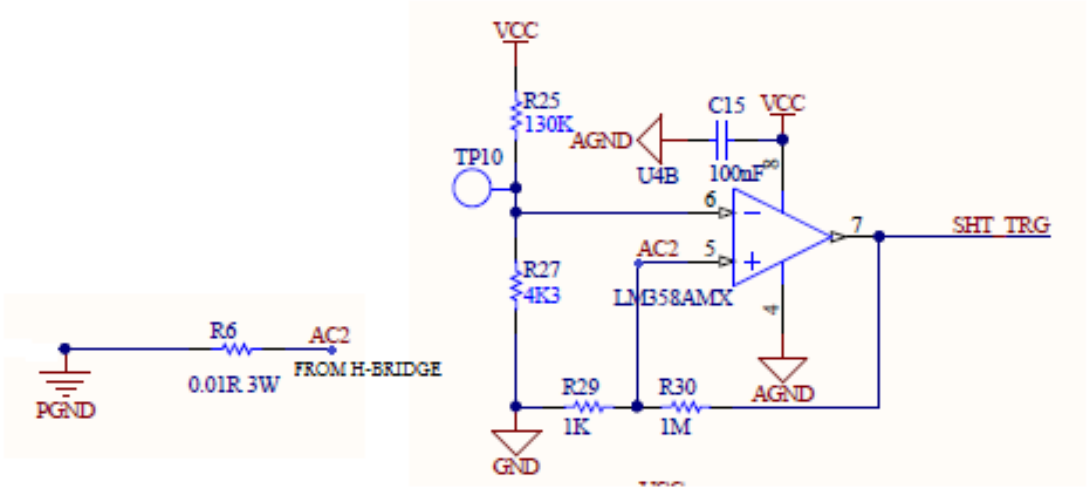


FIGURE 5.21: Implemented circuit for shoot-through protection.

Where $PGND$ Power ground, which taken as reference.

$AC2$ Point where the inverting terminal is connected to resistor for measuring voltage drop.

SHT_TRG Output which is fed to gate control circuitry.

TABLE 5.7: Operation truth table for shoot-through protection circuit

Mode	Reference Voltage	Input (*resistor*)	Op-Amp Output	Output after Inverting
Normal Operation	0.16V	$< 0.16V$	LOW	HIGH
Shoot Through	0.16V	$> 0.16V$	HIGH	LOW

When in normal operation, input to the non-inverting terminal will have a lower potential than that of the inverting one. The output from the comparator will be low. When a shoot through occurs, the potential at the non-inverting terminal will go high, and the output from the comparator will go high. This signal is passed through a NOT gate which inverts the signal. The output of the NOT gate will be high under normal operation and will be low during a fault. This will prevent the low side switching signals from reaching the gate driver, which will be discussed in detail in Section 5.3.5.

5.3.5 Gate Control Circuitry

This is the last stage in the control electronics, wherein the signals from microcontroller, 50 Hz Tracking and Shoot Through Protection circuit pass through the MOSFET gate control circuitry.

The gate control involves series of AND and NOT gate and buffers. This circuit generates four signals, in which high frequency signals are for the high side switches and low frequency (50 Hz) signals for the low side switches are given to the driver circuit. The gate control circuit and truth table for the Logical Circuit are given in Figure 5.22.The results obtained and waveforms are discussed in detail in Chapter 7

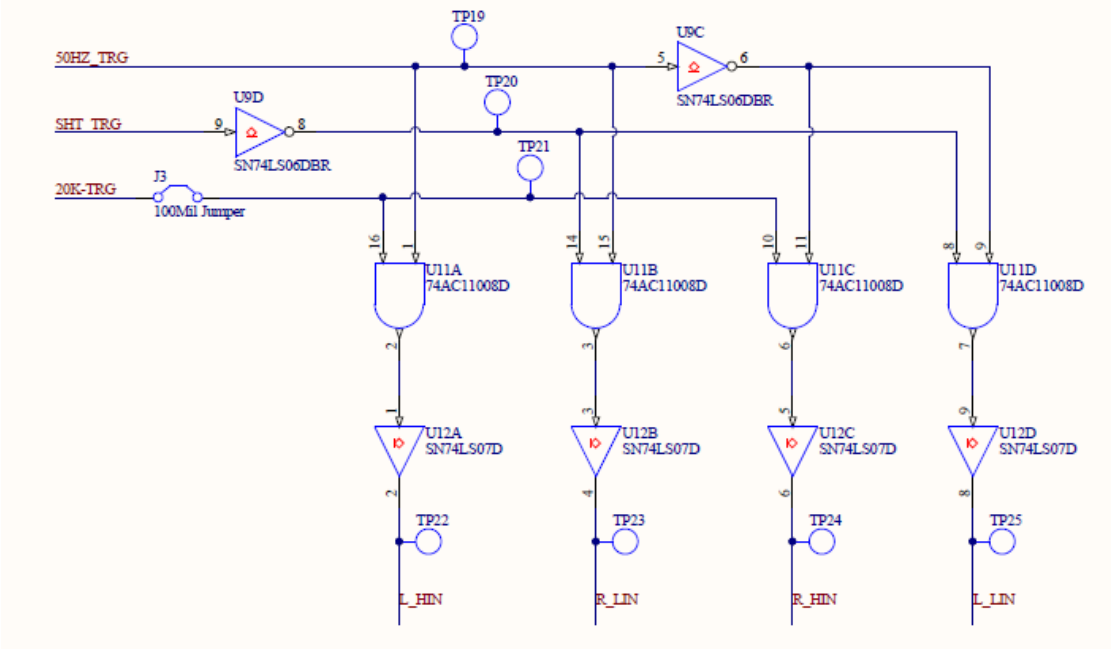


FIGURE 5.22: Logical circuitry implemented to obtain the gating signal.

Where	$50HZ\_TRG$	Switching signal for low side switches obtained from 50Hz tracking circuit.
	SHT_TRG	Trigger from shoot-through protection circuit.
	$20K-TRG$	High frequency PWM signal from microcontroller.
	L_HIN	Gate signal for high side switch Q1
	R_LIN	Gate signal for low side switch Q3
	R_HIN	Gate signal for high side switch Q2
	L_LIN	Gate signal for low side switch Q4

Refer to Appendix A for a detailed circuit of H-Bridge.

TABLE 5.8: Truth Table for gate control circuitry

Mode	$50HZ\_TRG$	SHT_TRG	TP-20	$20K-TRG$
Normal Operation	HIGH	LOW	HIGH	PWM
Normal Operation	LOW	LOW	HIGH	PWM
Shoot Through	HIGH	HIGH	LOW	PWM
Shoot Through	LOW	HIGH	LOW	PWM
Mode	Q1 (L_HIN)	Q3 (R_LIN)	Q2 (R_HIN)	Q4 (L_LIN)
Normal Operation	PWM	HIGH	LOW	LOW
Normal Operation	LOW	LOW	PWM	HIGH
Shoot Through	PWM	LOW	LOW	LOW
Shoot Through	LOW	LOW	PWM	LOW

5.4 Process Controller

5.4.1 Overview

An overall controller is required to measure system frequency, voltage and water heater cylinder temperature. A processor is also required to implement control algorithms, interface with the user and generate PWM signal.

TABLE 5.9: Different micro-controllers available and its features

Manufacturer	Series	Program Memory	RAM	Speed	Number of I/O pin
ATMEL	ATMega	32 Kbyte	1 Kbyte	20 MHz	23
Sypress Semiconductor	CY8C29xxx	32 Kbyte	2 Kbyte	24 MHz	44
Microchip	PIC16Fxxx	28 Kbyte	1 Kbyte	20 MHz	25
STMicroelectronics	STM8L15x	32 Kbyte	2 Kbyte	16 MHz	26

Since there are no complex computations, a cheap yet reliable controller can be chosen. Arduino-Uno board with Atmega 328p microcontroller has been chosen, considering the flexibility, cost of operation, ease of coding, etc.

The water heater control system has the following inputs:

1. Water heater cylinder temperature.
2. System voltage magnitude.
3. System voltage frequency.

4. User inputs.

The processor continuously controls the hot water element power based on these inputs.

5.4.2 Temperature Mode Of Operation

The temperature of the water inside the water heater defines whether the controller should operate or not. The region of operation is defined by two temperatures which are:

1. STEMP - Temperature limit corresponding to normal operation.
2. CTEMP - Cut-off temperature above which controller does not operate.

$STEMP$ and $CTEMP$ are initially programmed into the microcontroller. These parameters are not available for user to alter, but can be changed at the time of installation by changing the program code.

Figure 5.23 indicates the operating region of the controller with respect to the temperature of the water, where $STEMP$ and $CTEMP$ have been set as 65°C and 80°C by default. In the normal condition, the controller operates in the region $A-B-STEMP-O$. When the water in the heater is less than the set temperature, the controller is in the normal mode of operation, and the duty cycle of the high side switch is determined by the voltage and frequency at the time of operation, which will be discussed in detail in Section 5.4.3 and Section 5.4.4 respectively.

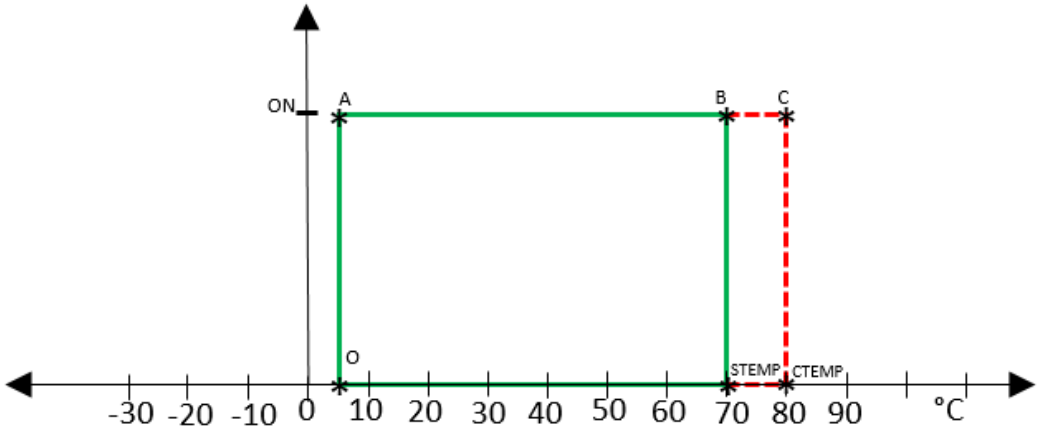


FIGURE 5.23: Plot describing the area of operation with respect to temperature.

The controller also has a programmed buffer so that energy can be dissipated under faulty conditions. This is indicated by the area $STEMP - B - C - CTEMP$. This

is set as a system reserve and it operates under critical conditions, when the frequency and voltage rise above the prescribed limits.

Operation in this area is expected when the water is fully heated up and there is a loss of load due to a fault in the grid. During this time, the controller runs at full duty cycle to utilise the excess power or a local over voltage in the grid. The water heater can act as a buffer/system reserve until the temperature of the water reaches $CTEMP$, above which it stops acting as a system reserve. The load is no longer available for management until the temperature is below the set temperature. If the fault is rectified during this time, the controller returns to the normal mode of operation.

5.4.3 Voltage Mode Of Operation

The voltage is measured using RMS to DC converters and taken into the microcontroller through analog port. A duty cycle profile is determined with respect to voltage.

From Figure 3.3 by using two point formula, the relation for duty cycle with respect to voltage is determined and the equation for the segment AB is given by

$$DC_v = \frac{(1 - DCV)(V_{mes} - V_1)}{V_2 - V_1} - DCV \tag{5.15}$$

Under normal operation, when the temperature of the water is less than the set temperature, the complete equation of the voltage profile is

$$DC_v = \begin{cases} 100\% & \text{if } V_{mes} > V_2 \\ \frac{(1-DCV)(V_{mes}-V_1)}{V_2-V_1} - DCV & \text{if } V_1 \leq V_{mes} \leq V_2 \\ 0\% & \text{if } V_1 < V_{mes} \end{cases}$$

Where	V_1	Lower voltage limit	(Volt)
	V_2	Upper voltage limit	(volt)
	V_{mes}	Measured voltage	(volt)
	DCV	Duty cycle corresponding to lower voltage limit	(%)

By default, the values for V1 , V2 and DCV are 210V, 240V and 25% respectively.

In conditions when the controller is operating as a system reserve, as mentioned in Section 5.4.2 the duty cycle is set to 100% and the above equations are not applicable. This is done so that a faster stabilization of the grid is achieved.

5.4.4 Frequency Mode Of Operation

The duty cycle is also dependent on frequency of the supply as frequency is affected by loss of generation or load in the national electricity supply system. Frequency is measured directly by microcontroller by using frequency measurement function with is discussed in Section 5.4.5.

From Figure 3.2 and again using the two point formula, the relation for duty cycle with respect to frequency is determined and the equation for the segment AB is given by

$$DC_f = \frac{(F_2 - F_1)(F_{mes} - F_1)}{DCF} \tag{5.16}$$

And for segment BC is given by

$$DC_f = \frac{(F_3 - F_2)(F_{mes} - F_2)}{100 - DCF} + DCF \tag{5.17}$$

Where	F_1	Lower frequency limit	(Hz)
	F_2	Intermediate frequency	(Hz)
	F_3	Upper frequency limit	(Hz)
	F_{mes}	Measured frequency	(Hz)
	DCF	Duty cycle corresponding to Intermediate frequency	(%)

By default, the values for F1, F2, F3 and DCF are 49.5 Hz, 50Hz, 50.5Hz and 50% respectively.

Under normal operation, when the temperature of the water is less than the set temperature, the complete equation of the frequency profile is

$$DC_f = \begin{cases} 100\% & \text{if } F_{mes} > F_3 \\ \frac{(F_3 - F_2)(F_{mes} - F_2)}{100 - DCF} + DCF & \text{if } F_2 \leq F_{mes} \leq F_3 \\ \frac{(F_2 - F_1)(F_{mes} - F_1)}{DCF} & \text{if } F_1 \leq F_{mes} \leq F_2 \\ 0\% & \text{if } F_1 < F_{mes} \end{cases}$$

In conditions when the controller is operating as a system reserve, as mentioned in Section 5.4.2, the above equations are not applicable and the duty cycle is set to 100%. This is also done so that a faster stabilization of the grid is achieved by increased power flow to the water heater element.

5.4.5 Processor Flow Chart

At start-up, the microcontroller is initialized and the high side gate driver output is pulled down to zero. The controller waits for 60 seconds during which its set key may be pressed. The microcontroller enters edit mode where the user can change the default parameters. If no key is pressed, the microcontroller retains the default values and proceeds with execution.

The microcontroller checks for the temperature of the water and determines whether the operating temperature is below STEMP or CTEMP and the corresponding flag is set. The microcontroller then measures the voltage and frequency using the built in analog to digital converter and frequency measuring function (fremeasure) respectively. A duty cycle corresponding to the measured voltage and frequency is determined as discussed in the Section 5.4.3 and 5.4.4. The microcontroller then checks for the status of the flag. A critical flag indicates that the water in the heater is above the critical temperature, above which it is not safe to operate.

The duty cycle is set to zero in this case. In the non-critical case, the microcontroller checks whether the flag is set. If the flag is set, the microcontroller checks whether the measured frequency and voltage are above the critical values, and if so the microcontroller is in the critical operating region as discussed in the previous section 5.4.2. If the measured voltage and frequency are below the critical values (i.e. there is no fault in the system and it is not an emergency situation) and if temperature of the water in the heater is at its maximum, duty cycle is set to zero. In the last case, when both flags are not set (i.e the water in the water heater has not reached the maximum), the microcontroller calculates the weighted duty cycle as per the equation 5.18.

$$DutyCycle = a.DC_f + b.DC_v \tag{5.18}$$

Where	Duty Cycle	Is the final duty cycle
	DC_f	Duty cycle corresponding to measured frequency
	DC_v	Duty cycle corresponding to measured voltage
		and a + b = 1 (Preference factor)

In cases where there is both under frequency and over voltage the controller checks for the preference factors and determine the operating region. The detailed operation mode selection is shown in Table 5.10

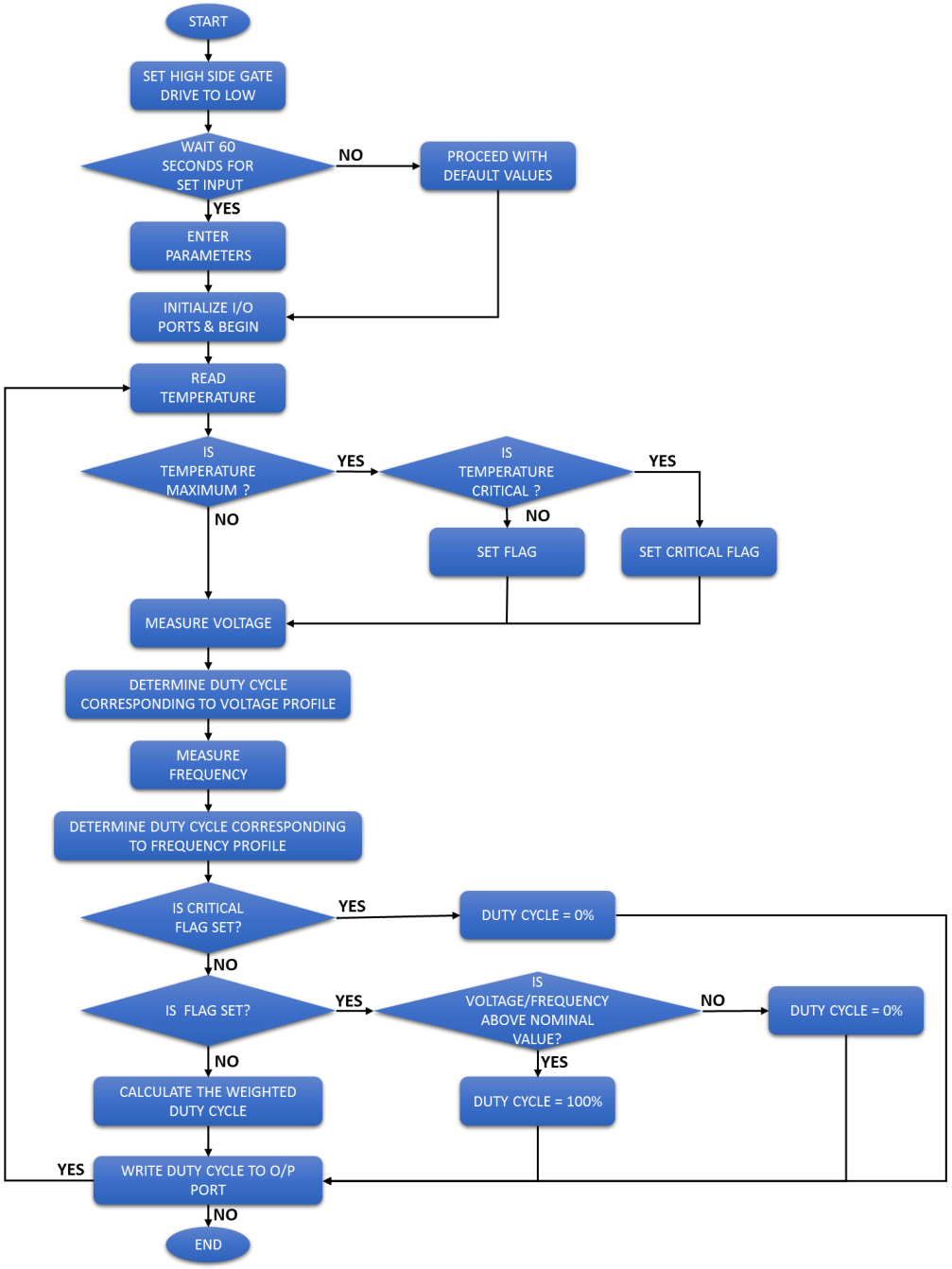


FIGURE 5.24: Flow chart for process controller.

The cycle repeats after the determined duty cycle is written to the output port.

TABLE 5.10: Different grid condition and its corresponding operationg regions

Voltage	Frequency	Water Temperature	Flag	Critical Flag	Preference factor (a)	Operating Region
Below Nominal	Below Nominal	Nominal, Maximum, Critical	Not Set, Set, Set	Not Set, Non Set, set	>0.5, 0.5, < 0.5	Duty Cycle 0%
Below Nominal	Nominal	Nominal, Maximum	Not Set, Set	Not Set	<0.5, 0.5	Duty Cycle 0%
Nominal	Below Nominal	Nominal, Maximum	Not Set, Set	Not Set	>0.5, 0.5	Duty Cycle 0%
Nominal	Nominal	Nominal	Not Set	Not Set	>0.5, 0.5, < 0.5	Normal Operation
Nominal	Nominal	Maximum, Critical	Set, Set	Not Set, Set	>0.5, 0.5, < 0.5	Duty Cycle 0%
Nominal	Above Nominal	Nominal, Maximum	Set	Not Set	>0.5, 0.5	Duty Cycle 100%
Nominal	Above Nominal	Critical	Set	Set	>0.5, 0.5	Duty Cycle 0%
Above Nominal	Nominal	Nominal, Maximum	Not Set, Set	Not Set	<0.5, 0.5	Duty Cycle 100%
Above Nominal	Nominal	Critical	Set	Set	<0.5, 0.5	Duty Cycle 0%
Above Nominal	Above Nominal	Nominal, Maximum	Not Set, Set	Not Set	>0.5, 0.5, < 0.5	Duty Cycle 100%
Above Nominal	Above Nominal	Critical	Set	Set	>0.5, 0.5, < 0.5	Duty Cycle 0%

Chapter 6

Mechanical Design

6.1 Overview

Any power electronic design is constrained by layout and power dissipation considerations. This chapter describes the thermal calculations for the circuit and the details of the heatsink and circuit board design.

6.2 Power Dissipation

Power dissipation is a key calculation which determines the physical layout of the final product. In this prototype, the power dissipation is mainly in three parts, as follows:

1. Power dissipation in the switches.
2. Power dissipation in the bridge rectifier.
3. Power dissipation in the 5V regulator. (Refer Appendix C)

6.2.1 Power Dissipation On MOSFET

The power dissipated by the MOSFET contributes to the major part of the losses. The power dissipation of a MOSFET includes the dissipation while conducting due to the on resistance and the switching losses (determined by the switching transition time and switching trajectory). The arrangement of switches is as shown in Figure 6.1.

6.2.1.1 Power Loss Due To ON Resistance

Every MOSFET when turned on will have an ON-resistance denoted by $R_{DS(ON)}$ which is specified in the data-sheet of the device. The loss due to $R_{DS(ON)}$ is also called conduction loss (P_{cond}).

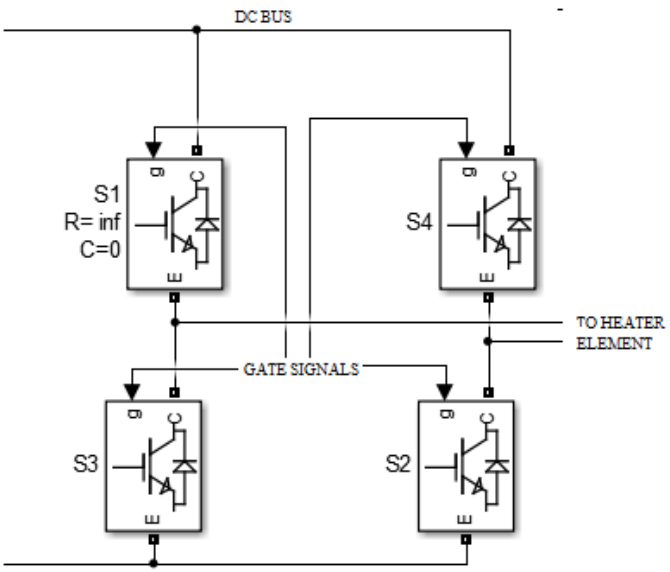


FIGURE 6.1: Arrangement of the MOSFET/IGBT in H-bridge configuration in Simulink.

$$P_{cond} = D * I_0^2 * R_{DS(ON)} \tag{6.1}$$

Where	P_{cond}	Conduction Loss.
	D	Duty Cycle
	I_0	Steady state current.
	$R_{DS(ON)}$	Source to drain ON resistance of MOSFET.

From Figure 6.2 we can notice that each pair of MOSFETs conducts only for a half cycle. The other distinguishing factor of this application is that the current is not constant. Therefore Equation 6.1 has to be modified for this application as:

$$P_{cond} = D * I_{rms}^2 * R_{DS(ON)} \tag{6.2}$$

Where	I_{rms}	rms value of current.

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (I_0 \sin^2 \omega t)^2 dt} \tag{6.3}$$

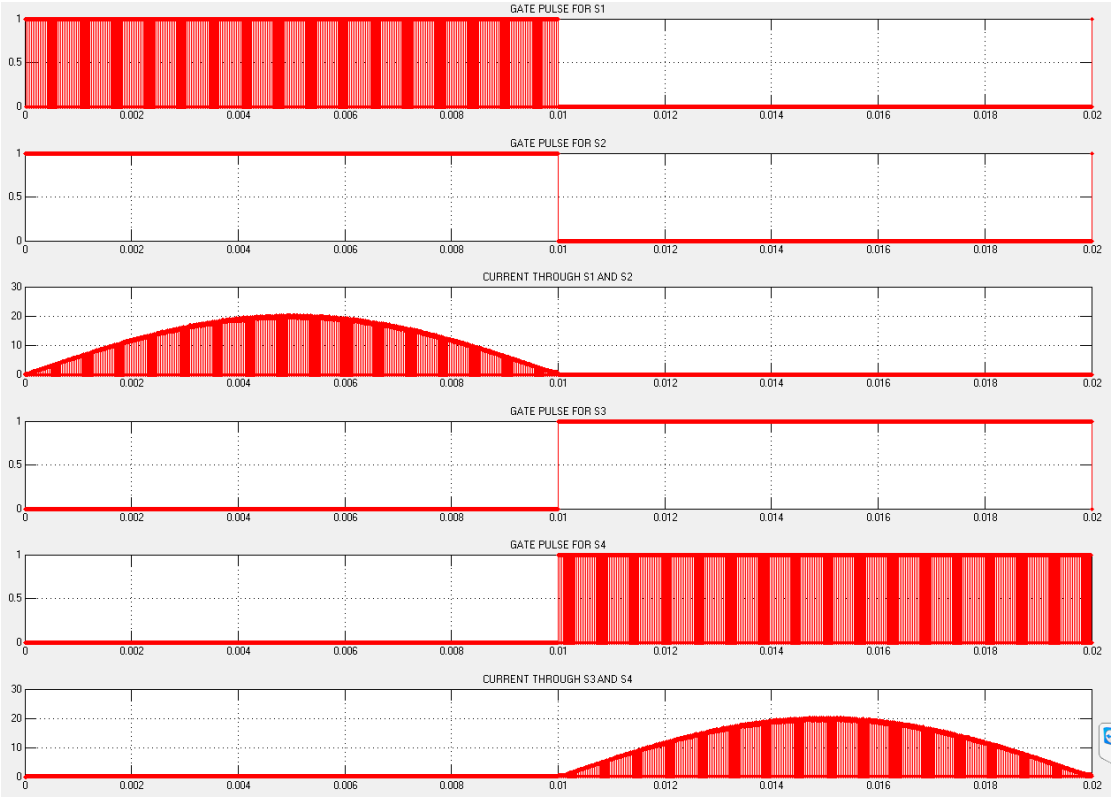


FIGURE 6.2: Wave forms showing the switching sequence and conduction current of various switches.

Considering the peak operating condition, at $350V_{(peak)}$ and heater element resistance of 16Ω, I_0 is calculated as 21.8A. From Equation 6.2 the rms current is calculated as 9.96A ≈ 10A. Substituting the values in Equation 6.3, at 95% duty cycle and $R_{DS(ON)}$ 0.13Ω, the losses in MOSFET FDP26N40 is calculated to be 12 Watts. The worst case is when MOSFET is on all the time, i.e at 100% duty cycle is 13 Watts

Since MOSFET S1 and S2 conduct together the dissipation will be same for both. Similarly for S3 and S4 the dissipation would be the same. Therefore the total dissipation due to $R_{DS(ON)}$ on all four MOSFETs is up to 48 Watts.

6.2.1.2 Power Loss Due To Switching

The other source of power loss is through switching losses. As each MOSFET switches and during switching, it carries both voltage and current. The losses are proportional to the switching frequency and the values of the parasitic capacitances and the switching time. As the physical size of the MOSFET increases, its switching speed decreases. Increasing MOSFET size also increases the switching loss.

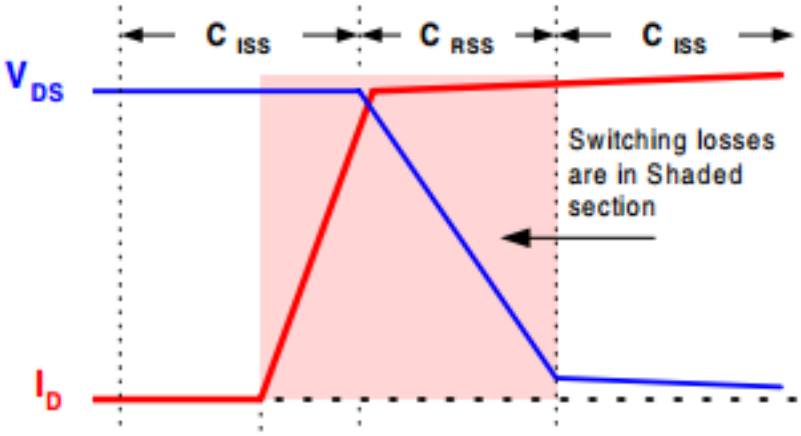


FIGURE 6.3: Graph showing the switching loss in a MOSFET[36].

As per Fairchild application note AN-6005, the switching losses can be determined from the following equation:

$$P_{switch} = \frac{(V_{DS}I_D)(t_{ON} + t_{OFF})F_{sw}}{2} \tag{6.4}$$

Where	P_{switch}	Power dissipation during switching.
	V_{DS}	DC bus rail voltage (Drain to Source voltage).
	I_D	Drain current or steady state current.
	t_{ON}	Turn ON (Rise time)time of MOSFET.
	t_{OFF}	Turn OFF (Fall time)time of MOSFET.
	F_{sw}	Switching frequency of MOSFET.

From the datasheet of FAN26N40, t_{ON} and t_{OFF} are obtained as 100ns and 66ns respectively. Taking $V_{DS(rms)}$ as 250V, which is the maximum possible rail voltage and $I_{D(rms)}$ as 10A, at 31kHz switching loss for the high side switches S1 and S4 is 6.4 Watts.

From Figure 6.4 it can be seen that S1 and S4 do not switch all the time. The average power dissipation would be half the calculated value, i.e 3.2 Watts each.

The switching losses in the lower side switches S2 and S3 can be neglected. From Figure 6.4 it can be seen that the MOSFETs S2 and S3 switch at voltage current zero crossings. Since rail voltage is zero at the time of switching, power dissipation due to switching is also zero.

The total dissipation in four switches is 54.4 Watts.

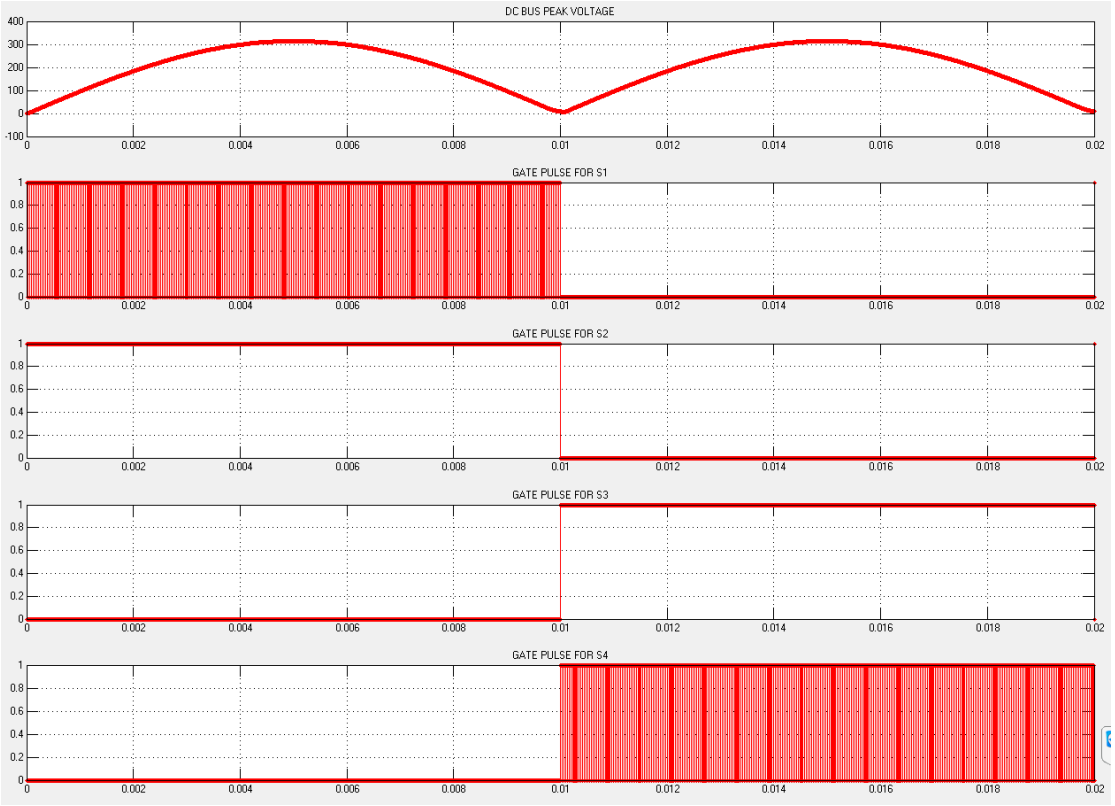


FIGURE 6.4: Waveforms showing the switching sequence and DC bus voltage.

6.2.1.3 Power Dissipation Due To Bridge Rectifier

The bridge rectifier in the power stage also dissipates power like every other device. The dissipation in a bridge rectifier is due to the forward voltage drop (V_f) of the bridge. The dissipated power can be calculated according to the Equation 6.5.

$$P_{bridge} = 2 * V_f * I_f \tag{6.5}$$

Where	P_{bridge}	Power dissipation during conduction.
	V_f	Forward voltage drop.
	I_f	Forward conduction current.

From the datasheet of bridge rectifier PB3006, V_f is noted to be 0.97V. The power dissipated at 16A is 31 Watts. Adding a safety margin to it the power dissipated is approximated to 35 Watts. The graph depicting power dissipation with respect to forward current is as shown in Figure 6.5.

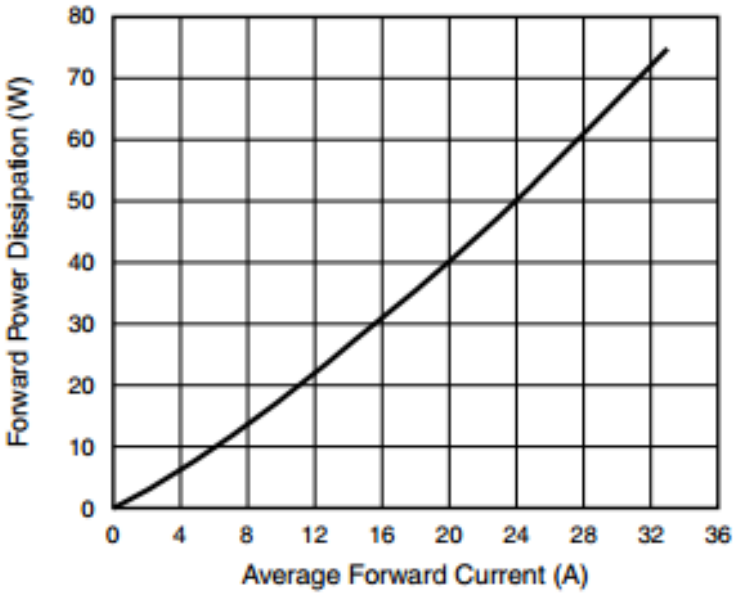


FIGURE 6.5: Graph showing power dissipation versus forward current[42].

6.3 Heat sink design

Once the power dissipation of various devices are determined the heat sink design is the next design stage. Parameters of the heat sink determine the form factor and PCB layout.

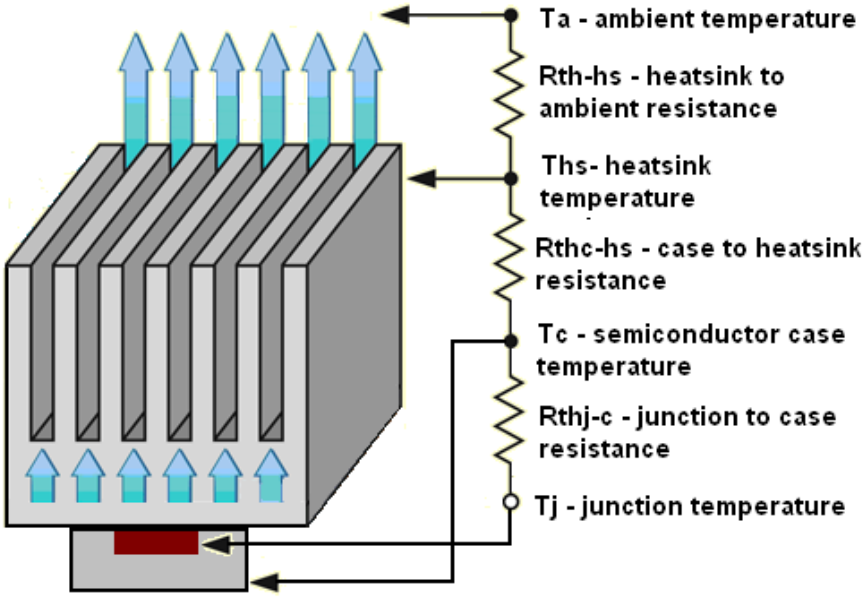


FIGURE 6.6: Figure depicting thermal resistance[43].

The equation for computing the steady state heat sink values are:

$$T_j = P * (R_{jc} + R_{cs} + R_{sa}) + T_a \tag{6.6}$$

Where T_j Junction temperature.
P Power dissipation.
R_{jc} Thermal resistance junction to case.
R_{cs} Thermal resistance case to sink ($0.7 - 0.9°C/W$ for insulation pad with thermal paste)
R_{sa} Thermal resistance sink to ambient.
T_a Ambient temperature.

The bridge rectifier and the MOSFET are connected to seperate heatsinks due to the mechanical constraint in desiging the PCB (refer Appendix A for PCB layout). The sink to ambient thermal resistance (R_{sa}) for the MOSFET and bridge rectifier is calculated as shown in Table 6.1.

TABLE 6.1: Heat sink availability and cost comparison

Device	P (W)	T_j $Typ(Max)$ (°C)	R_{jc} ($°C/W$)	R_{cs} ($°C/W$)	T_a (°C)	R_{sa} $(Calculated)$ ($°C/W$)
MOSFET	55	125 (150)	0.6	0.8	25	0.41
Bridge Rectifier	35	125 (150)	0.95	0.7	25	1.2

In the worst case scenario when MOSFET is conducting all the time the total power dissipated by the MOSFETs is 59 Watts. With the above calculated R_{sa} of $0.41°C/W$ the junction temperature T_j is 132°C, well under the maximum temperature of 150°C.

Various heat sinks were considered and it was concluded that an extruded block heat sink would be the right choice compared to modular ones. Since the heat sink is naturally cooled it has to be mounted on the outside surface of the box containing the PCB which will be discussed in Section 6.4.

Wakefield-Vette 510-9M heat sink was selected for its low cost with low thermal resistance at $0.29°C/W$. For details of the heat sink refer Appendix C. The heat sink was cut into the required dimension, thereby keeping the thermal resistance within the calculated limits.

TABLE 6.2: Heat sink availability and cost comparison

			Thermal Resistance		
Manufacturer	Part No.	Case style	Natural Convection ($°C/W$)	Forced Convection ($°C/W$)	Price Per Unit (NZD)
H S MARSTON	07WN-01500-A-200	Module	1.5	NA	33.06
AAVID THERMALLOY	D180-20	Extruded Block	0.33	0.045	328.60
SEMIKRON	P3/300B	Extruded Block	0.33	NA	193.87
H S MARSTON	96CN-03000-A-200	Extruded Block	0.28	NA	235.19
FISCHER ELEKTRONIK	SK 56/ 200 SA	Extruded Block	0.3	NA	153.66
WAKEFIELD-VETTE	510-9M	Extruded Block	0.29	0.066	146

6.4 PCB Design

The next step was to design a PCB for the circuits discussed in Chapter 5. A polycarbonate water sealed box manufactured by Rose Bopla (part no.091224100) is used to contain the PCB. The box and the lid together are of dimension $240mm \times 120mm \times 100.5mm$ ($Length \times Breadth \times Height$) and rated for IP66 & NEMA 4X standards. The PCB is limited to these internal dimensions.

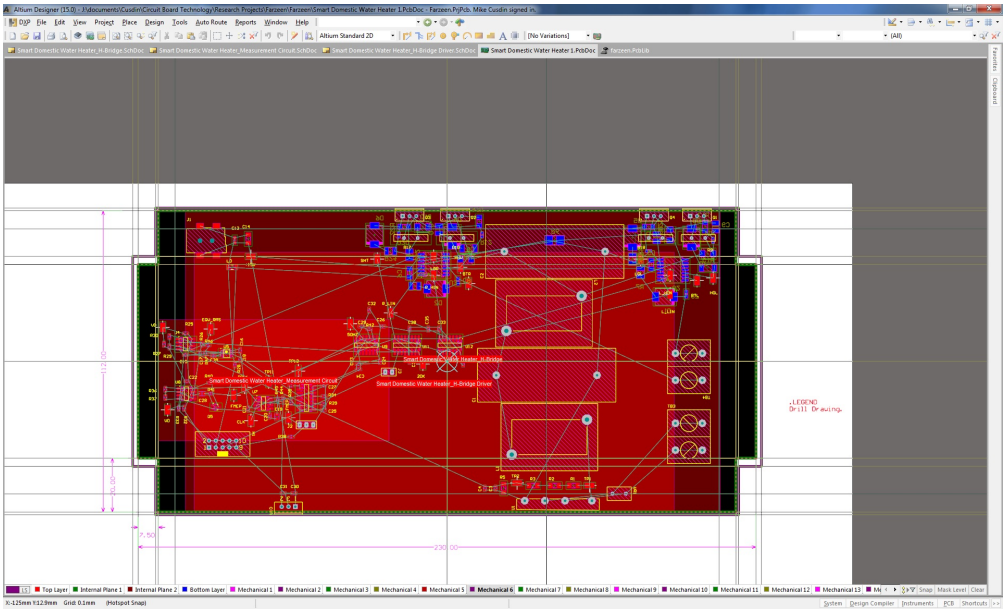


FIGURE 6.7: Altium designer 15

Now that the maximum PCB board outline is determined, the PCB can be designed. Altium Designer 15 software package was used for drawing schematics and for the design of the PCB. Initially schematics were prepared and verified. After finalizing the schematics, PCB layout and design were done. Figure 6.7 shows the PCB designing in Altium Designer.

Design and Application notes suggest many parameters, which were taken into account during the design[44]. Recommendation for PCB design:

1. Two separate ground planes; one plane for control signals and second plane for power which is connected to -ve or ground. These help to avoid the effect of switching ($\frac{di}{dt}$) on the control signal.

2. Simplest and most effective method of noise suppression is to have separate grounding for analog and digital portions of circuitry as shown in Figure 6.8.

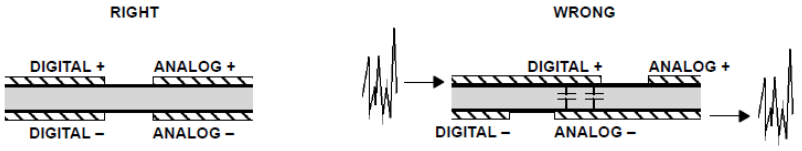


FIGURE 6.8: Layout of planes[44].

3. Dividing the PCB into seperate digital, analog and power sections with separate ground planes would be the best. Figure 6.9 shows an example of good layout.

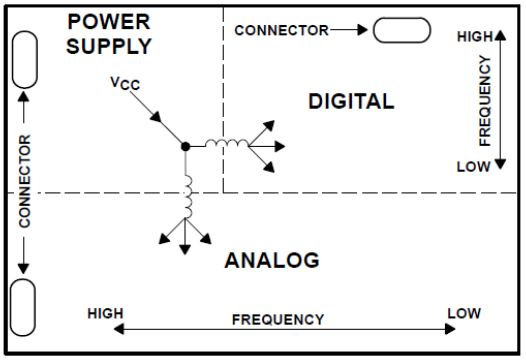


FIGURE 6.9: Layout of planes[44].

4. Trace corners are to be made as smooth as possible in order to avoid sharp and 90° bends in tracks. Figure 6.10 shows various trace corners.

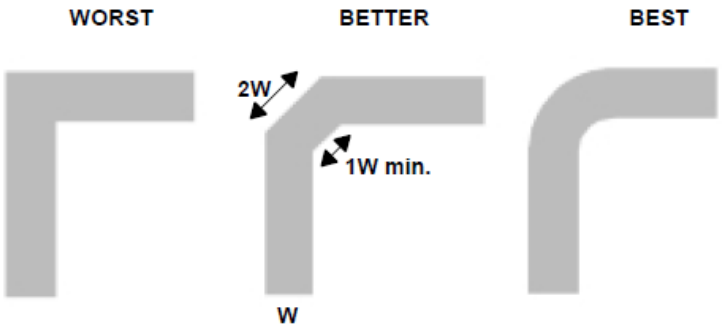
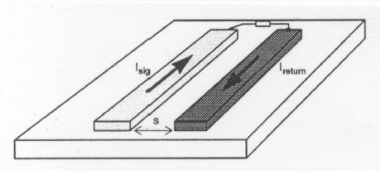
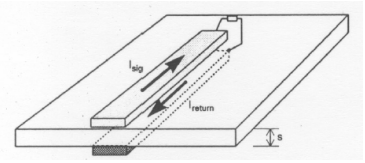
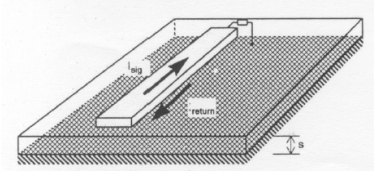


FIGURE 6.10: PCB Trace corners[44].

5. Lowering the package height of MOSFET above PCB, straightening the tracks between gate drive & MOSFET gate with minimum loops & interconnection are recommended as these add significant inductance.

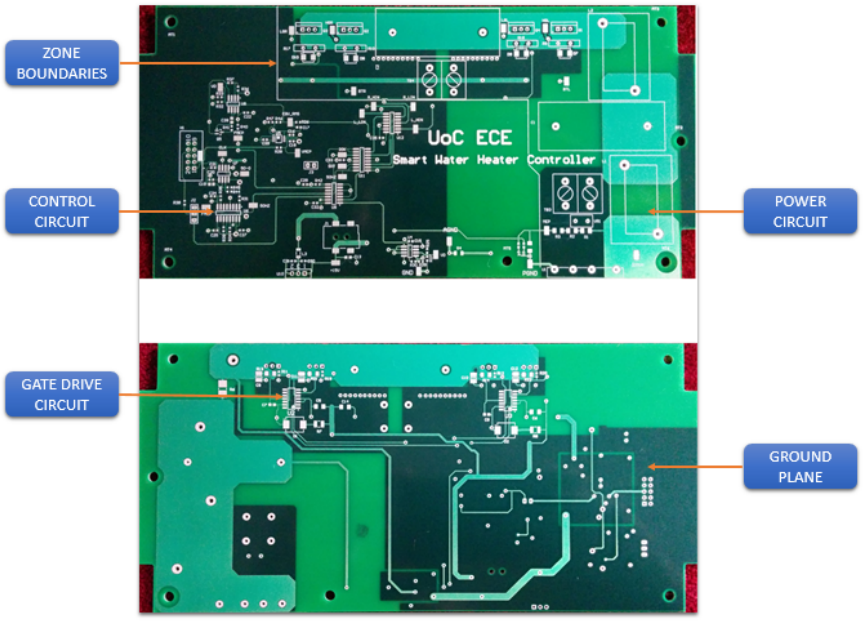
6. Co-locating the power MOSFET to reduce track length, placing of decoupling capacitor & gate resistor close to gate drive IC and placing the bootstrap diode close to bootstrap capacitor can reduce the parasitic inductances.

TABLE 6.3: Various layout of PCB tracks[45].

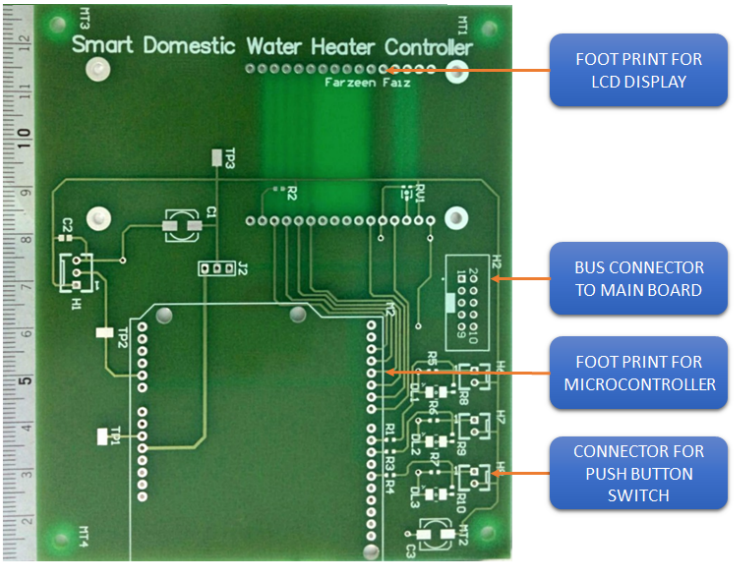
Path	Circuit	Description
Parallel Tracks		The forward path and return path are laid parallel to each other. The overall loop inductance is determined by the separation S between the track. Skin effect will be maximum in this case.
Tracks on opposite side		In this case the return path is on the opposite side of the forward path. The separation between the track, S in this case is the thickness of the PCB.
Ground Plane		Here a ground plane is used on one of the layers of PCB. The ground plane allows return path for any track above ground plane.

The operation of the sensitive control electronics could be affected by the high current switching on the power board. Hence, radiated EMI from the power PCB must be considered. Since there was a relatively low cost difference between the two layer and four

layer board, it was considered preferable to use a four layer PCB to allow a dedicated power ground shield to be placed on the bottom layer of the control PCB. The components were placed by dividing the PCB into power circuit, control electronics and gate drive circuit regions.



(A) Main PCB.



(B) Processor PCB

FIGURE 6.11: 4 layer PCB board.

Figure 6.11 depicts the final board after construction. The main PCB in Figure 6.11A contains the power circuit, gate drive circuit and the control circuit. The processor controller board in Figure 6.11B contains the microcontroller, LCD display, bus connector and the mounts for push button switches.

Chapter 7

Circuit Testing

7.1 Overview

This chapter describes the circuit testing that has been achieved to date. As the control method is not completely straightforward, firstly the control circuit itsself is demonstrated. Following this the gate drive circuit operation is confirmed, and then some limited testing of the full circuit under load is presented. Due to time limitations full power circuit testing wasn't acheived, so a final simulation of the circuit operation is presented.

1. Control and measurement circuit.
2. Gate drive circuit.
3. Complete system.
4. Final simulation.

7.2 Control and measurement circuit

The control circuit has several key tasks. Firstly has to provide signals to switch the two lower switches in the bridge at 50Hz, synchronised with the 50Hz mains voltage. Secondly, it generates a 31kHz PWM control signal based on system measured frequency and voltage, and directs this PWM signal to the switch that is diagonaly opposite to the lower switch that is in ON state.

The control circuit is a very important part of the project, since it measures the input parameters and generates the gate signals for the gate driver. It has to be checked thoroughly before it is integrated into the system. A test rig as shown in Figure 7.1 was set up for testing the control circuit. Since the control circuit is tested independently,

the rectified voltage signal from the DC Bus which is used by the control circuit is not available. A secondary circuit has been used to generate the input signal.

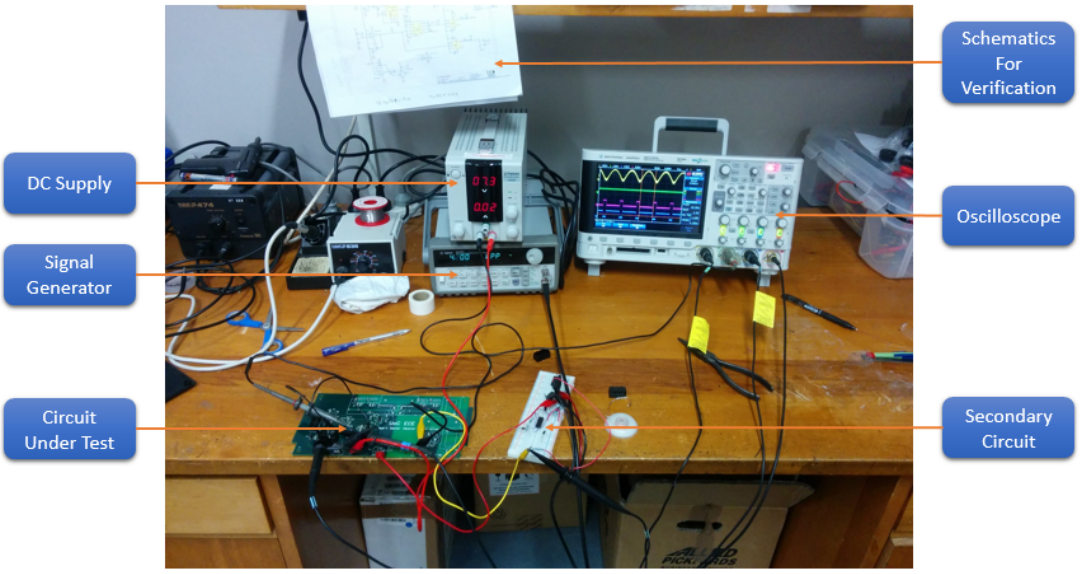


FIGURE 7.1: Test rig for testing of control circuit.

A signal generator has been used to generate $5V_P$ sinusoidal wave of 50 Hz, which was rectified and fed into the control circuits.

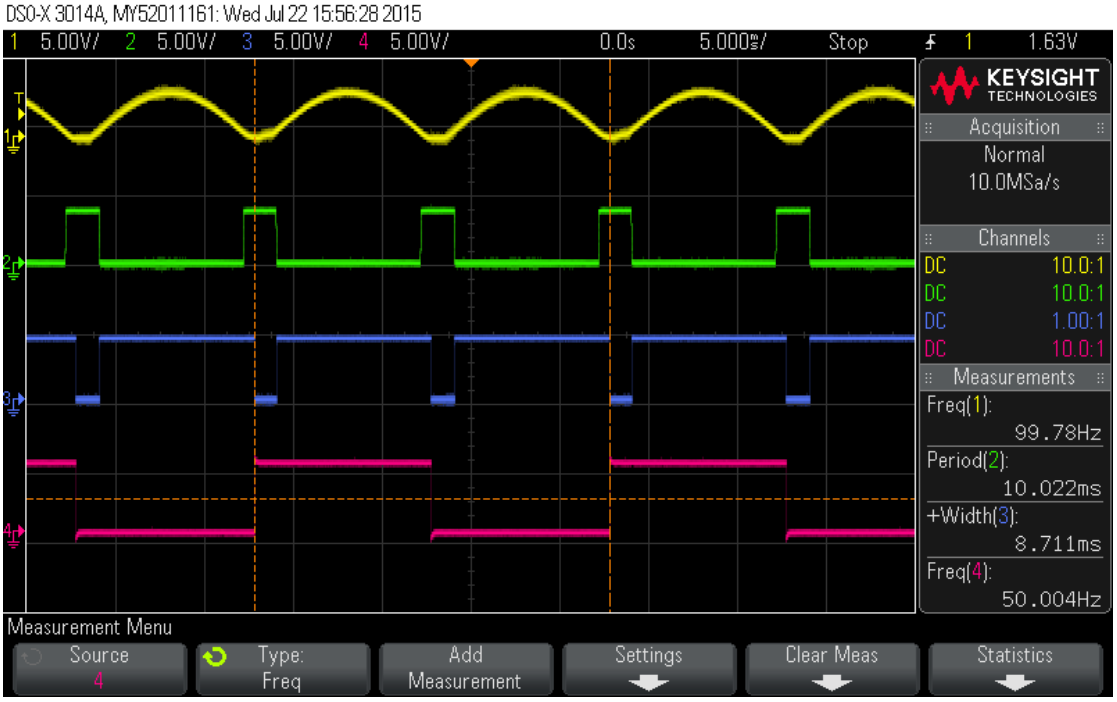
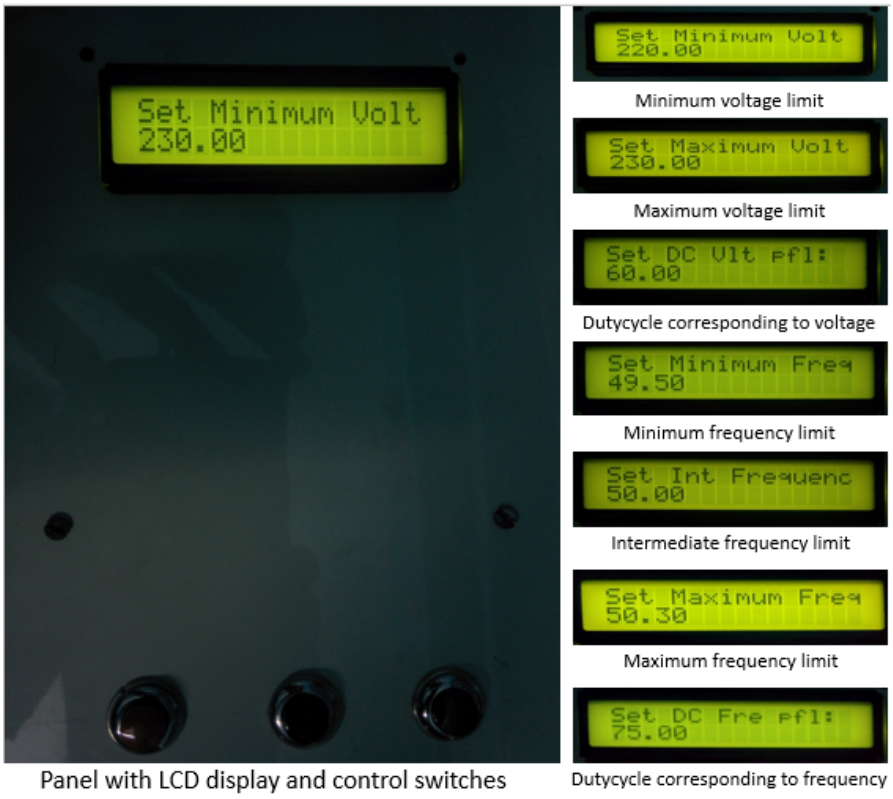
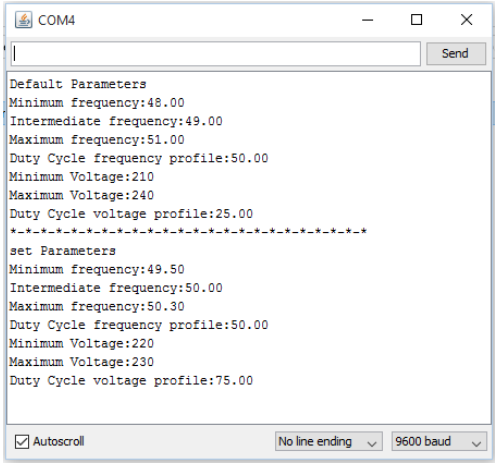


FIGURE 7.2: Waveforms obtained during testing of control circuit.

Figure 7.2 shows the waveform obtained. Channel 1 (*yellow*) is the rectified 50Hz AC signal obtained from the secondary circuit. Channel 2 (*green*) shows the output of the comparator level detector which is used to synchronise the 50Hz switching signal with the grid frequency. Output of the 555 timer circuit is shown in channel 3 (*blue*), the falling edge marks the zero crossing point of the rectified AC wave. The timer circuit was designed for 9 ms but the output shows the ON time as 8.71ms, this was due to the tolerance of the R and C values used.



(A) Parameters being initialized



(B) Default and initialized parameter

FIGURE 7.3: Initialization of parameters.

The output of the 555 timer is given to a J-K flip-flop in toggle state. The 50 Hz signal which is used to switch the lower switches at zero crossing is obtained in channel 4 (*pink*), i.e the output of the flip-flop.

After testing the 50Hz switching signals, the microcontroller and software were tested. The signals obtained from the control circuit were used as input signals.

The microcontroller has to be initialized and the required parameters as discussed in Section 5.4.5 are manually entered.

Figure 7.3 shows user interface. Three push button switches (up, down, set) are used to adjust the parameters. Figure 7.3 shows the initial system parameters. The default parameters that are used in the absence of set button-press in the first 60 seconds after the controller has been turned ON and the parameters that have been initialized can be accessed using the serial communication port as shown in Figure 7.3.

The grid frequency switching of the MOSFET is fixed in hardware, however the 31kHz PWN is set by the microcontroller, based on system frequency and/or voltage as per Chapter 5. The variation of duty cycle with respect to voltage and frequency was studied independently to analyze the performance and resolution.

Figures 7.4 to 7.6 shows the variation of duty cycle with respect to voltage.

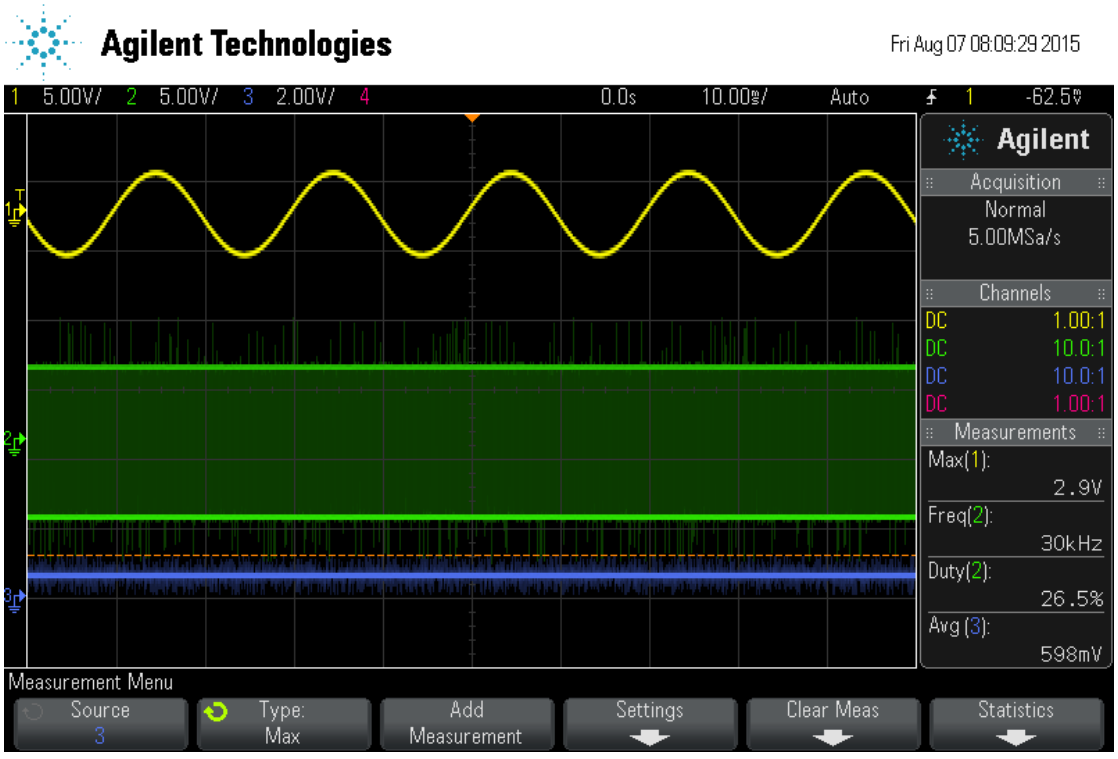


FIGURE 7.4: Duty cycle at 210V

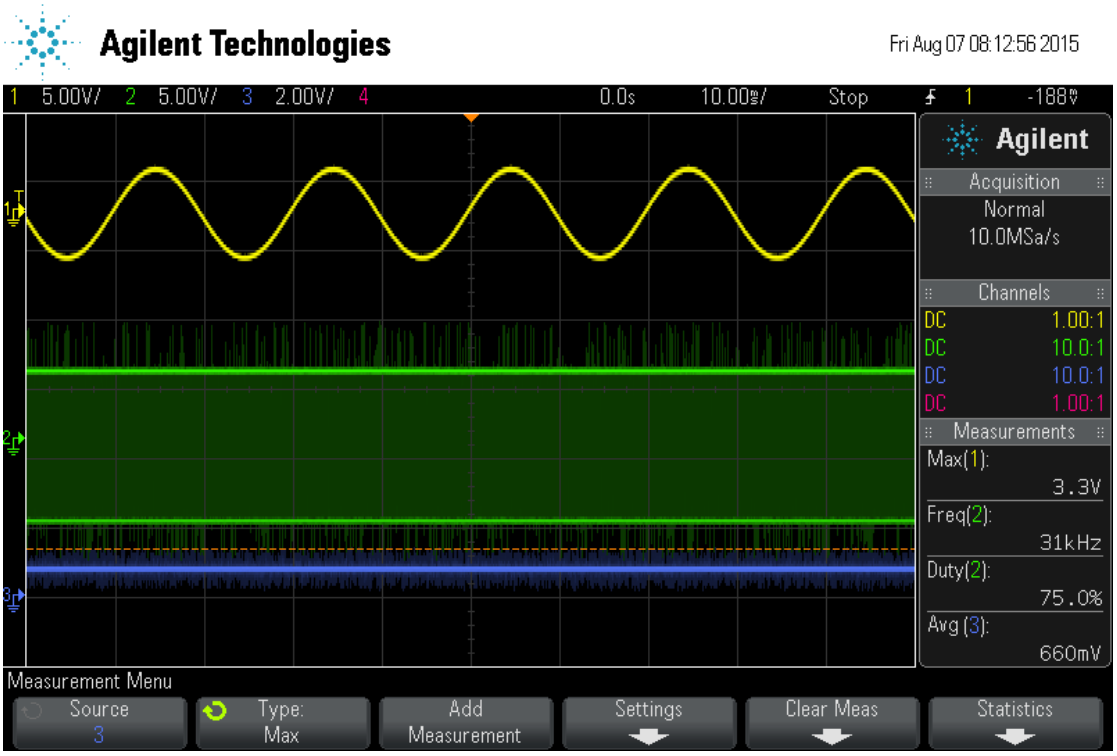


FIGURE 7.5: Duty cycle at 230V

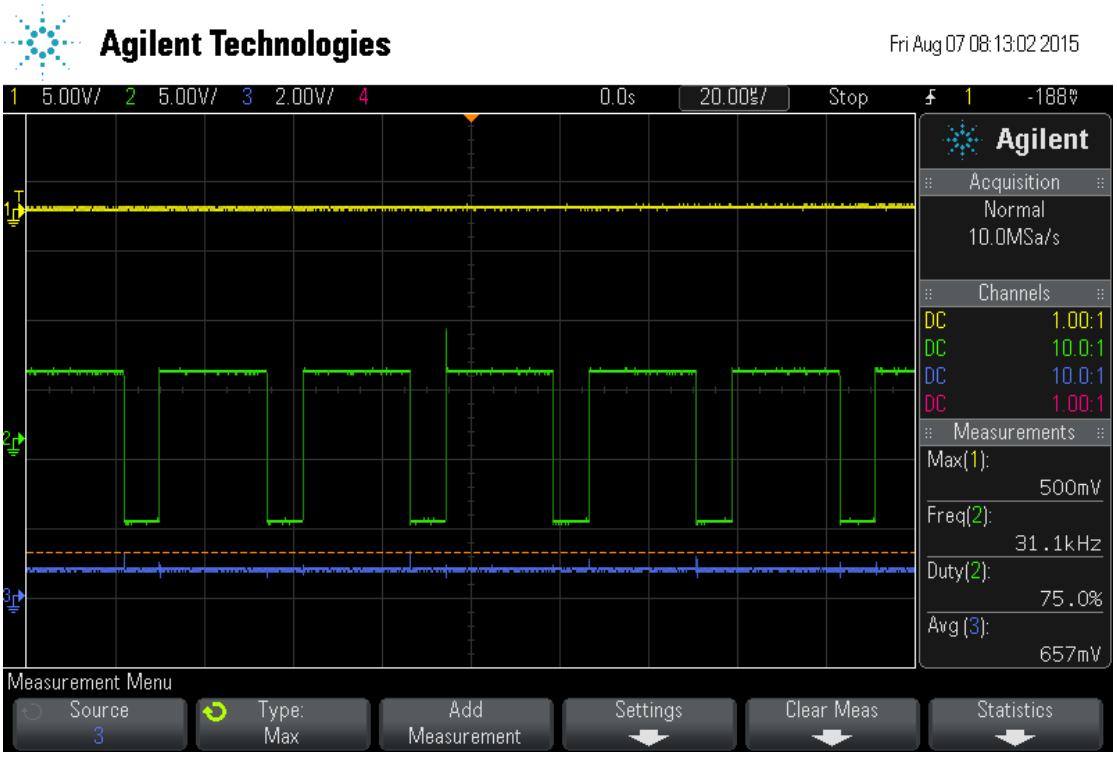


FIGURE 7.6: Enlarged time scale view for duty cycle at 230V

In Figure 7.4 to 7.6 channel 1 (*yellow*), channel 2 (*green*) and channel 3 (*blue*) show the stepdown AC signal, PWM output of the microcontroller and the output of the RMS

to DC converter. The calibaration of the voltage measurement was programmed in the microcontroller.

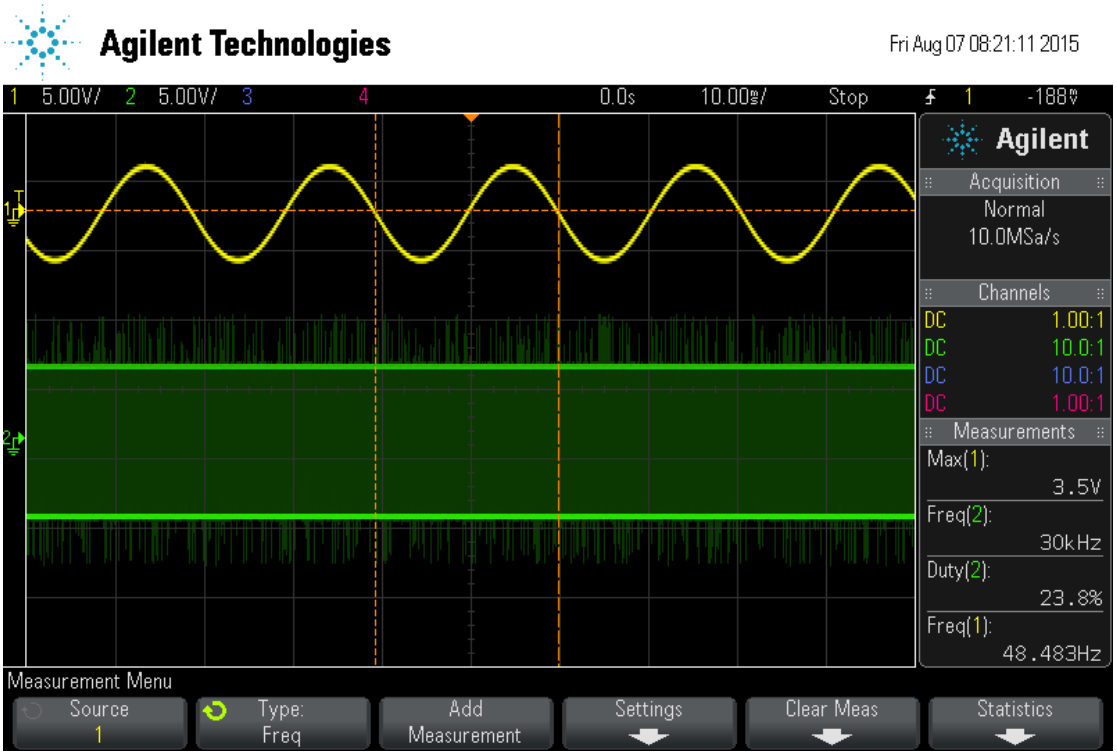


FIGURE 7.7: Duty cycle at 48.5Hz

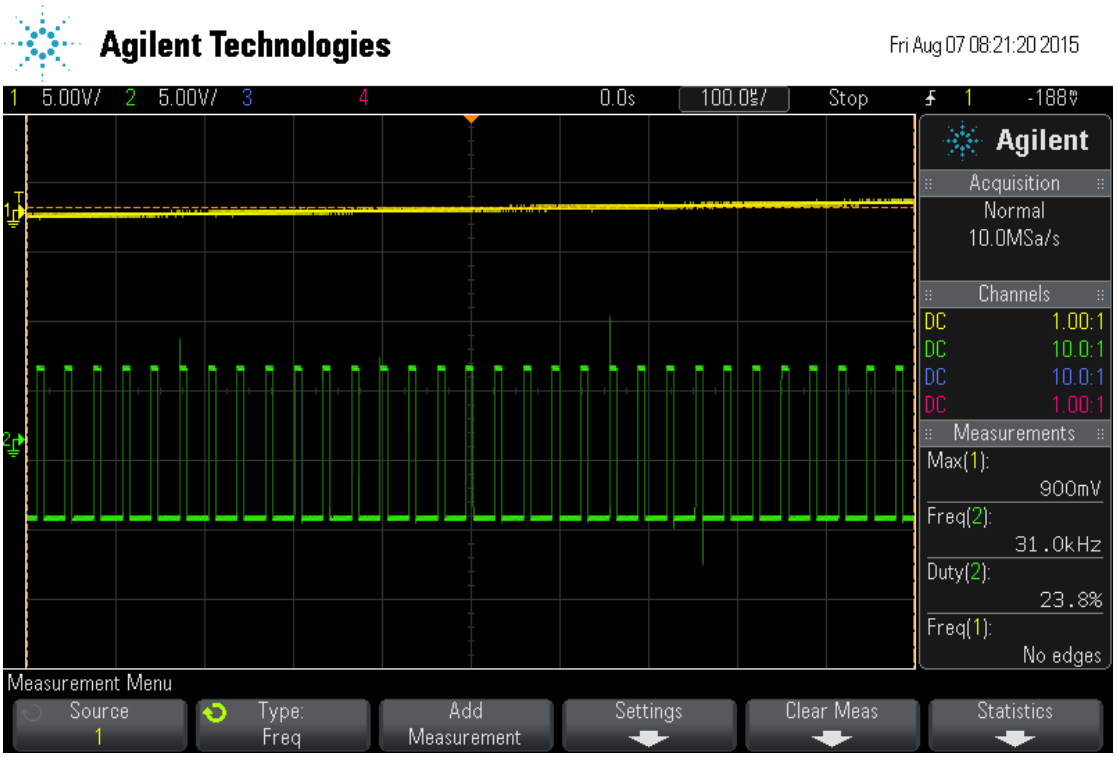


FIGURE 7.8: Duty cycle at 49.5Hz

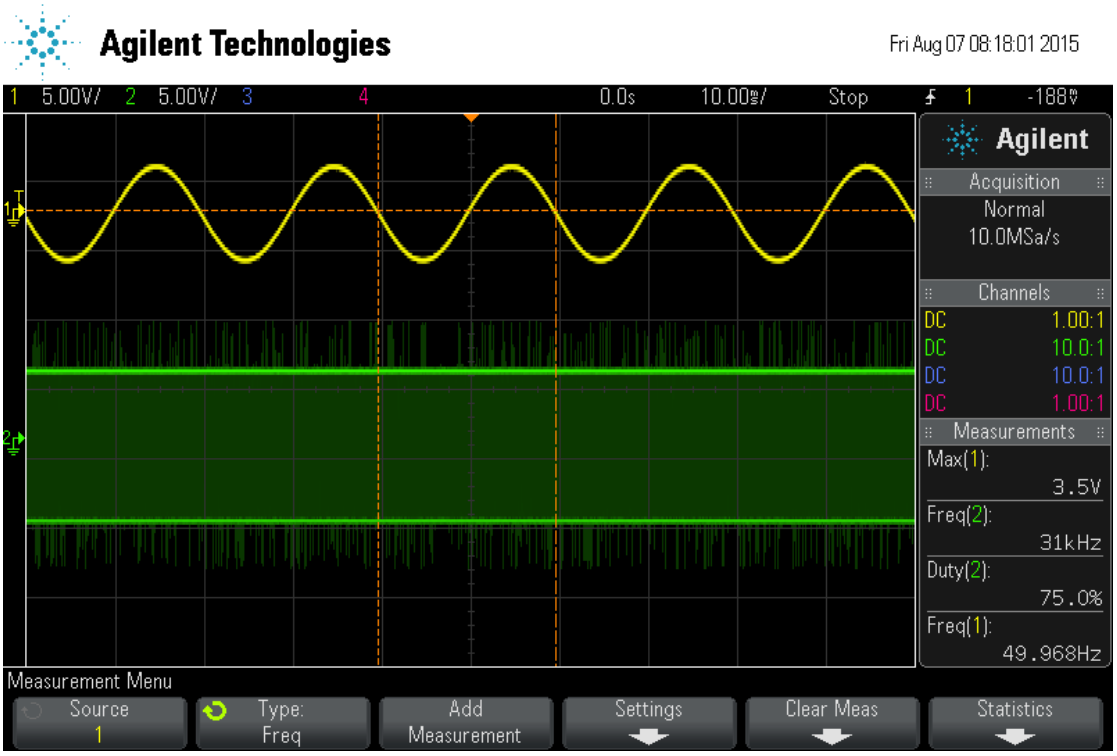


FIGURE 7.9: Duty cycle at 50Hz

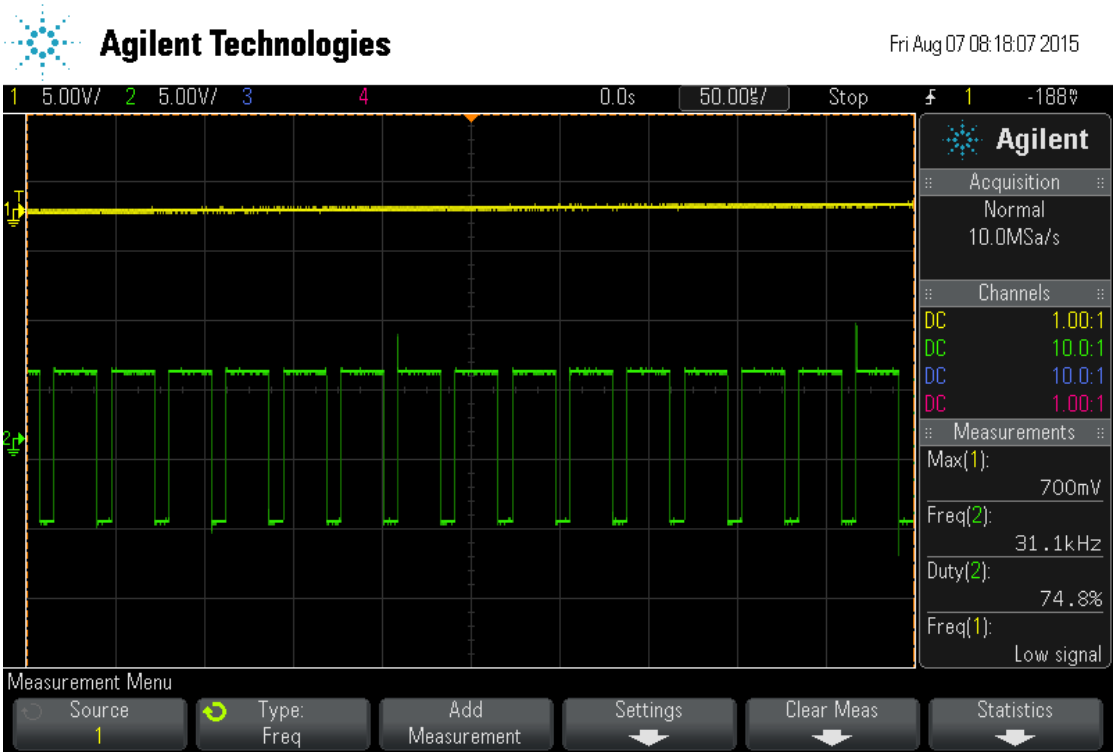


FIGURE 7.10: Duty cycle at 50Hz

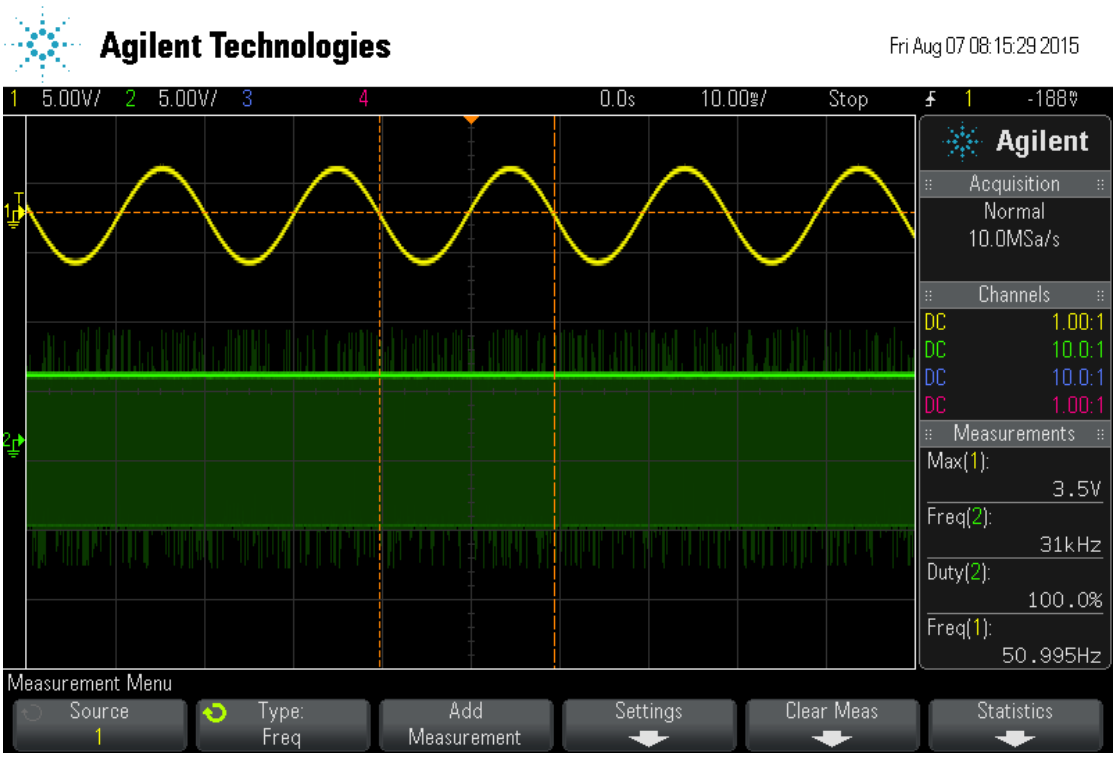


FIGURE 7.11: Duty cycle at 51Hz

Figure 7.7 to 7.11 shows the variation of duty cycle of the PWM output of microcontroller with change in frequency of the input AC signal. Channel 1 and channel 2 show the stepped down input AC signal and PWM output of the microcontroller respectively. The variation of the duty cycle with respect to frequency profile is can be noted.

7.3 Gate Drive Testing

After obtaining the 50Hz and PWM switching signal from the control circuit and the microcontroller respectively, the gate control circuitry was tested. The four signals (L_LIN, L_HIN, R_LIN and R_HIN) required to drive the gate drive circuit were obtained.

The output of the gate control circuit is shown in Figure 7.12. Channel 1 (*yellow*) and channel 4 (*pink*) are the left side gate control signal L_LIN and L_HIN respectively. The right side gate control signal R_LIN and R_HIN are shown in Channel 2 (*green*) and channel 3 (*blue*) respectively. Refer Appendix A for detailed circuit and signal labels. In this case the PWM switching frequency is limited to 600Hz so that both the PWM and 50Hz switching is visible. All the switching signal show a rapid rise and fall between 0V and 6V.

As discussed in Chapter 5, the interfacing of the gate control circuit to MOSFET switches was done by the Bootstrap gate drive circut. The driver circuit was tested and the input and output wave forms were studied.

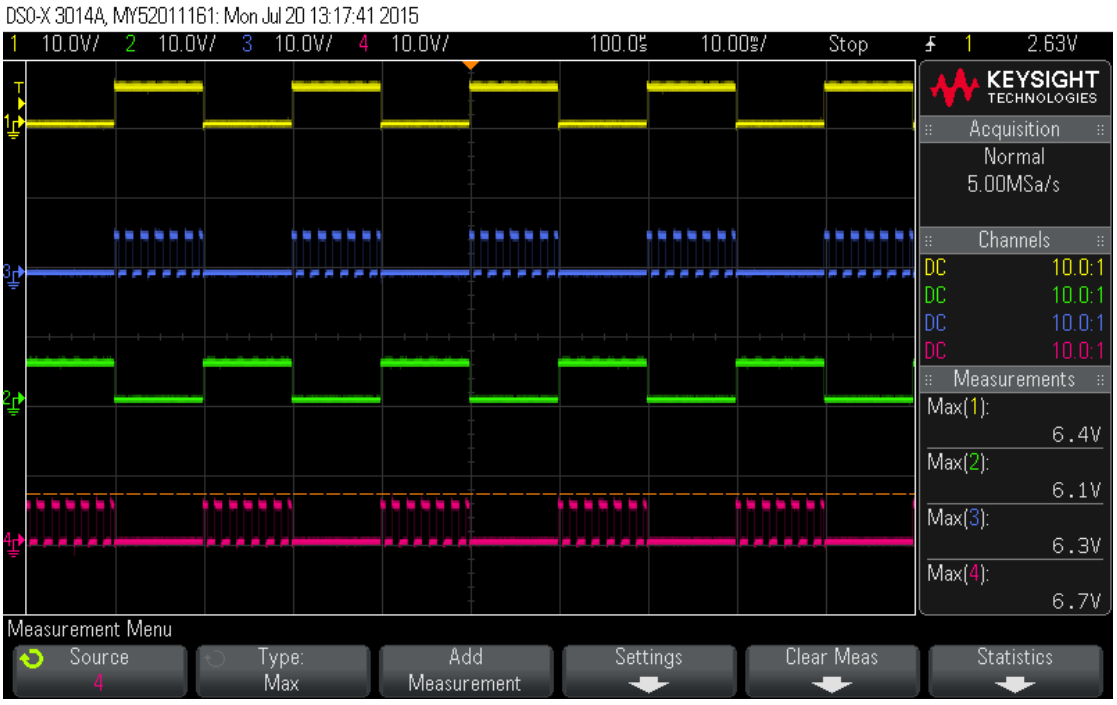


FIGURE 7.12: Output of the gate control circuit.

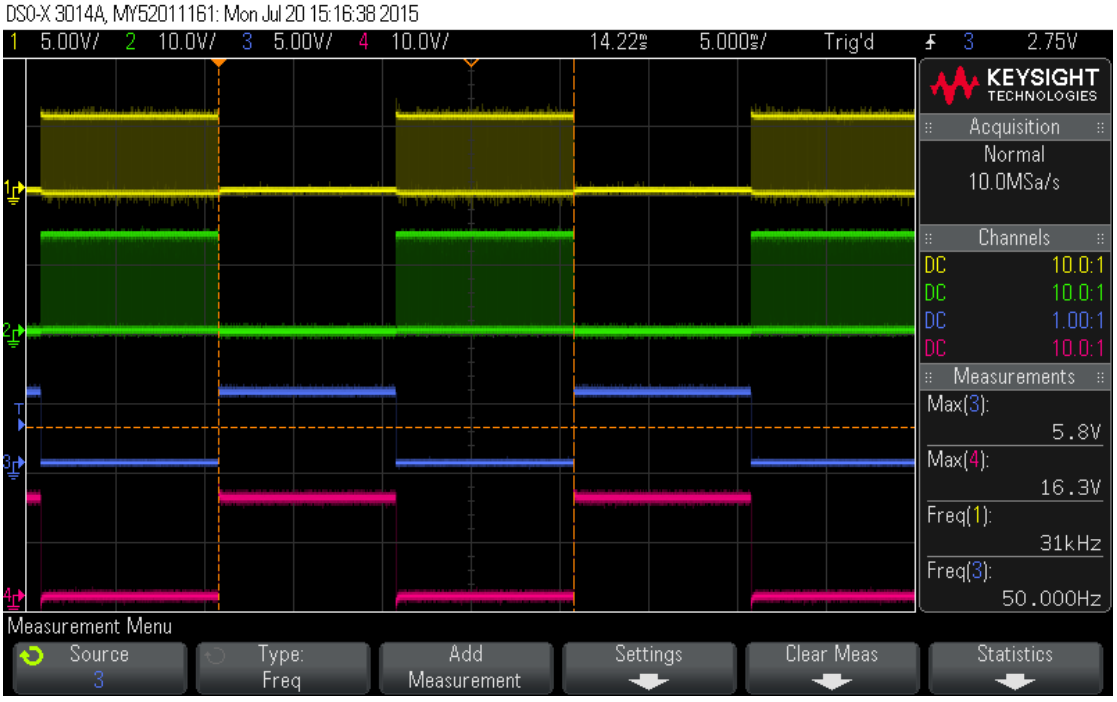


FIGURE 7.13: Input and output of boot-strap circuit.

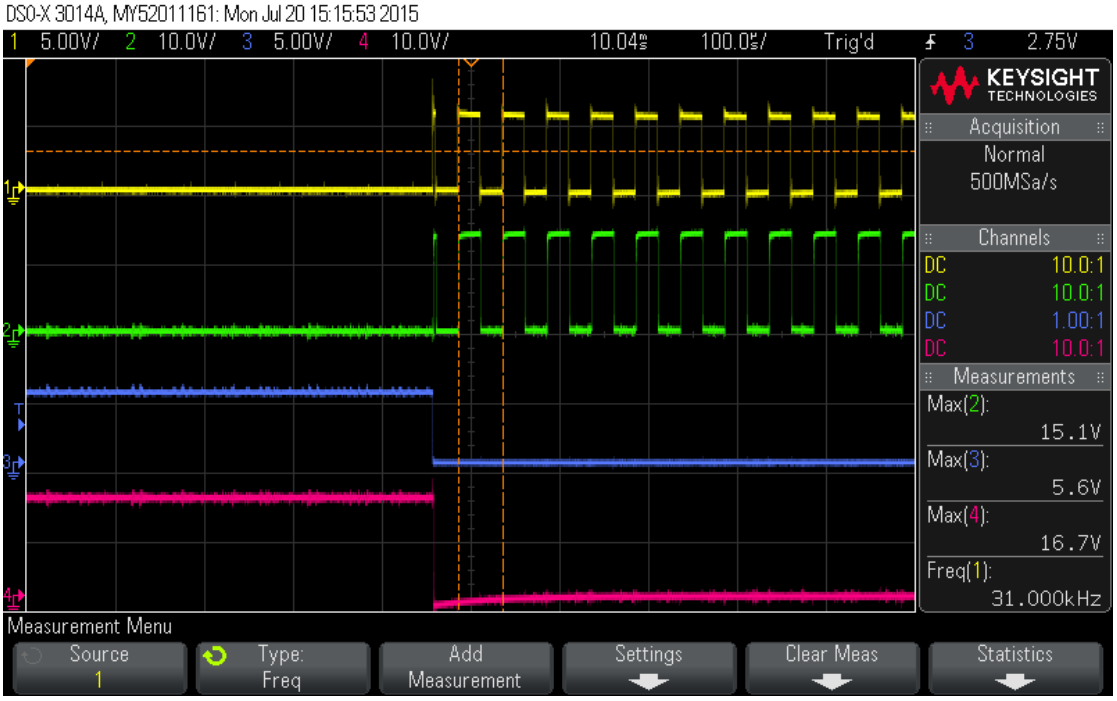


FIGURE 7.14: Enlarged time-scale input and output of bootstap circuit.

Figure 7.13 and 7.14 shows the comparison of the input to output of bootstrap circuit. Channel 1 (*yellow*) is the input (L_HIN) at 5V and 31kHz and Channel 2 (*green*) is the output which is connected to gate of MOSFET Q1 (refer Appendix A), signal is at 15V and 31kHz. Channel 3 (*blue*) and channel 4 (*pink*) show input (L_LIN) and bootstrap output to MOSFET Q4 respectively. It can be noted that when MOSFET Q1 is ON MOSFET Q4 is in OFF state, this is required gate signal as MOSFET Q1 and Q4 are on the same side of the H-Bridge.

The drive signals to the gates of MOSFETs Q3, Q1, Q4 and Q2 are obtained in channel 1 (*yellow*), 3 (*blue*), 2 (*green*) and 4 (*pink*) respectively are shown in Figure 7.15. The bootstrap gate drive IC (Fairchild FAN73933) used has programmable dead time, which can be changed by placing a series resistor between DT (pin 4) and ground. In this case default dead time of 220ns was maintained by directly connecting to ground. Refer Appendix A for circuit details.

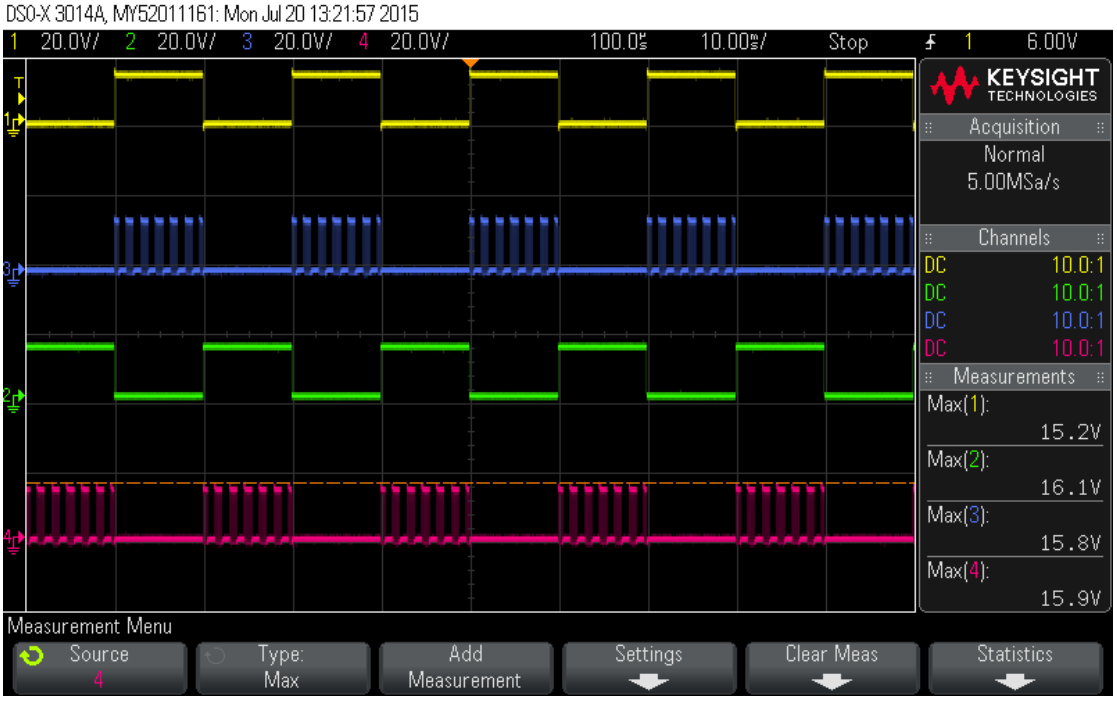


FIGURE 7.15: Output of boot-strap circuit to gate of MOSFETs.

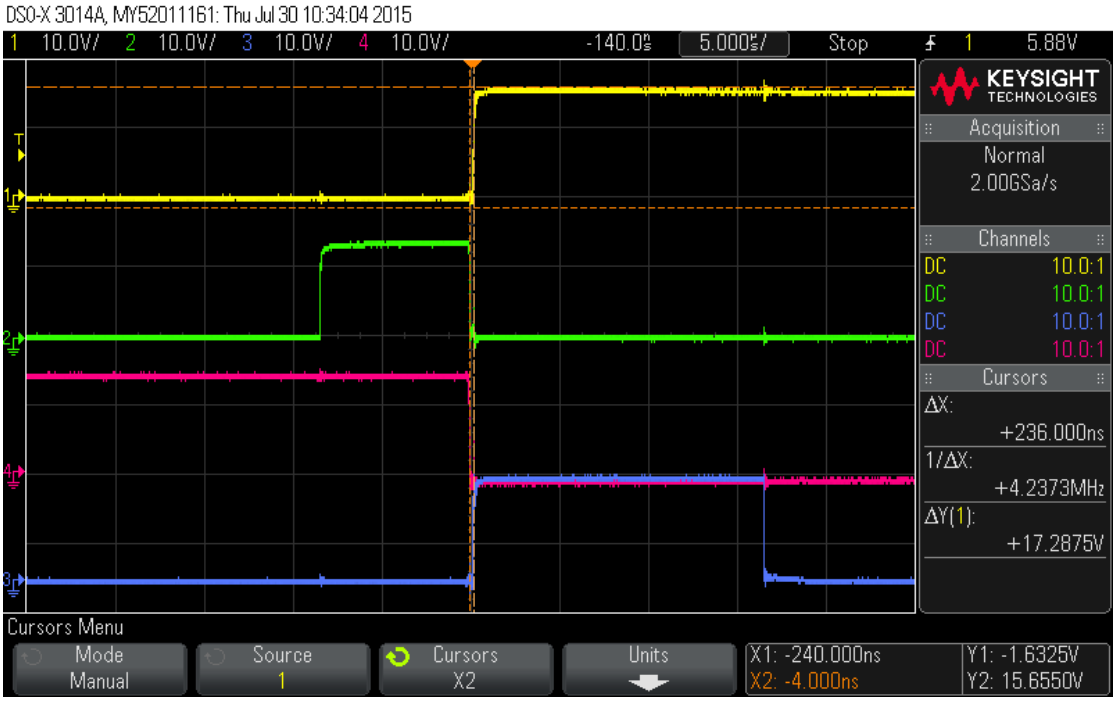


FIGURE 7.16: Dead time between switching.

Figure 7.16 shows the measured dead time of 236ns between high side and low side switching. Channel 1 & 2 being the gate signals to the MOSFET Q4 & Q1 which are on the left hand side of the H-bridge and Channel 3 & 4 being the gate signals to the MOSFET Q2 & Q3 which are on the right hand side of the H-bridge.

7.4 Complete System Testing

Once all the individual circuit in the system were tested independently and proved to be working, the blocks were put together and tested. The test rig is shown in Figure 7.17.

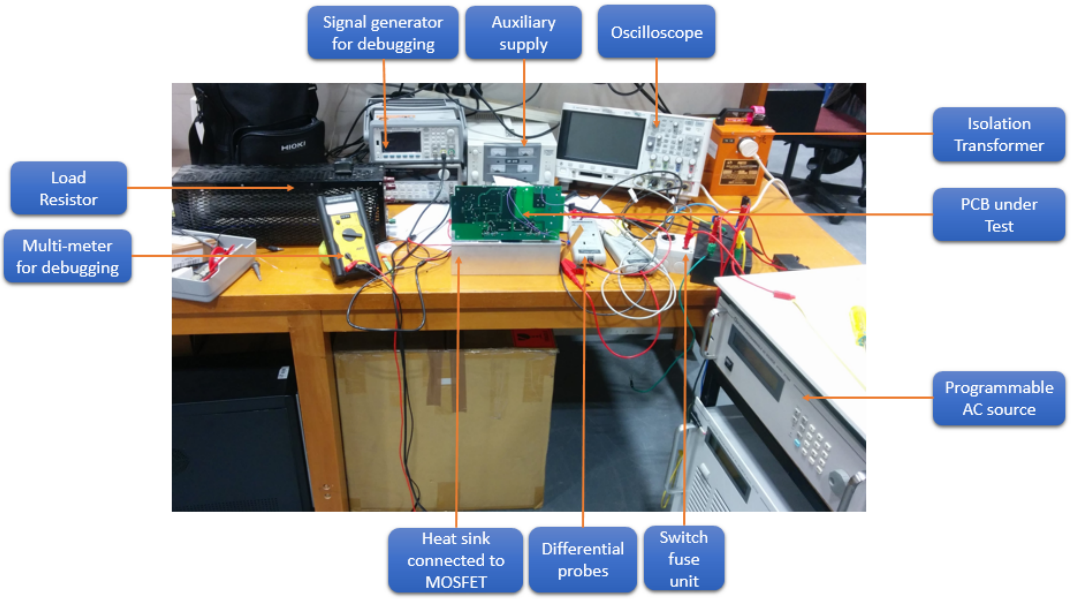


FIGURE 7.17: Complete test rig.

Figure 7.18 shows the voltage waveform across load resistor. A differential probe was used to measure the voltage across the load and normal probes connected between gate and ground were used to analyse the working of bootstrap circuit. Channel 1 & 2 in Figure 7.18 clearly shows the bootstrapping, the gate to ground voltage is gate-drive circuit supply (16V) added to the rail voltage (100V) (i.e $V_{g-ground}$ is V_{rail} + $V_{DD(bootstrap)}$). The distorsion of voltage waveform accross the load due to rectifier discontinuous conduction (RDC), discussed in Chapter 5 can be clearly seen in channel 4 in Figure 7.18. The expected output is a sinisoidal voltage waveform with a fundemental fequnecy of 50Hz.

The system was tested at 100V AC input with 3Kω 1A rheostat at 75% duty cycle. Figure 7.18 shows the wave forms obtained.

Due to time constrain the prototype couldn't be tested again with the revised filter design. Thus the following waveforms which were not able to produce from prototype-1 were obtained in Simulink:

1. AC side current waveforms.

2. Voltage waveforms across the load.

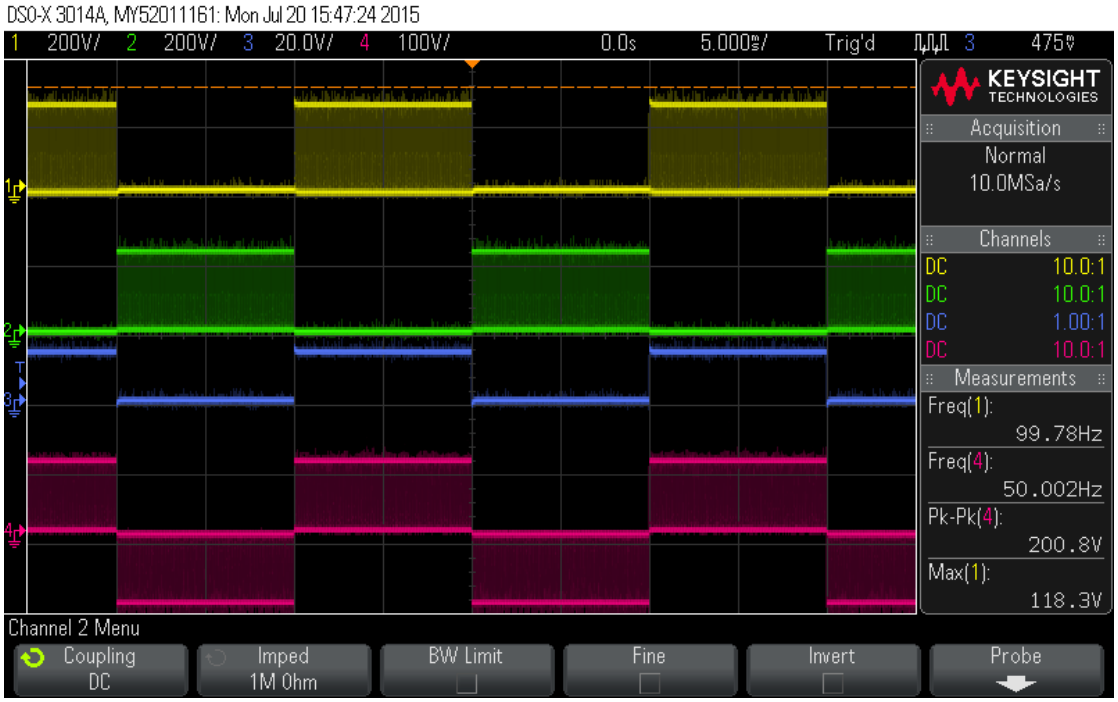


FIGURE 7.18: Waveforms obtained in complete system test.

7.5 Final Simulation

In order to study the ac side harmonics and to do further analysis of filter effectiveness, MATLab simulation was done. The simulation was done with the observations and results obtained during the testing phase. Initially the filter was re-designed and the new LC filter was tested for various duty cycles in order to check for discontinuous conduction of rectifier. A duty cycle of 25% was set as minimum, (as discussed in Chapter 5) and LC filter was re-designed. The simulation suggests a 200μH inductor and 1.2μF capacitor would eliminate the problem of RDC for duty cycle above 25%. Figure 7.19 shows the MATLab simulation model.

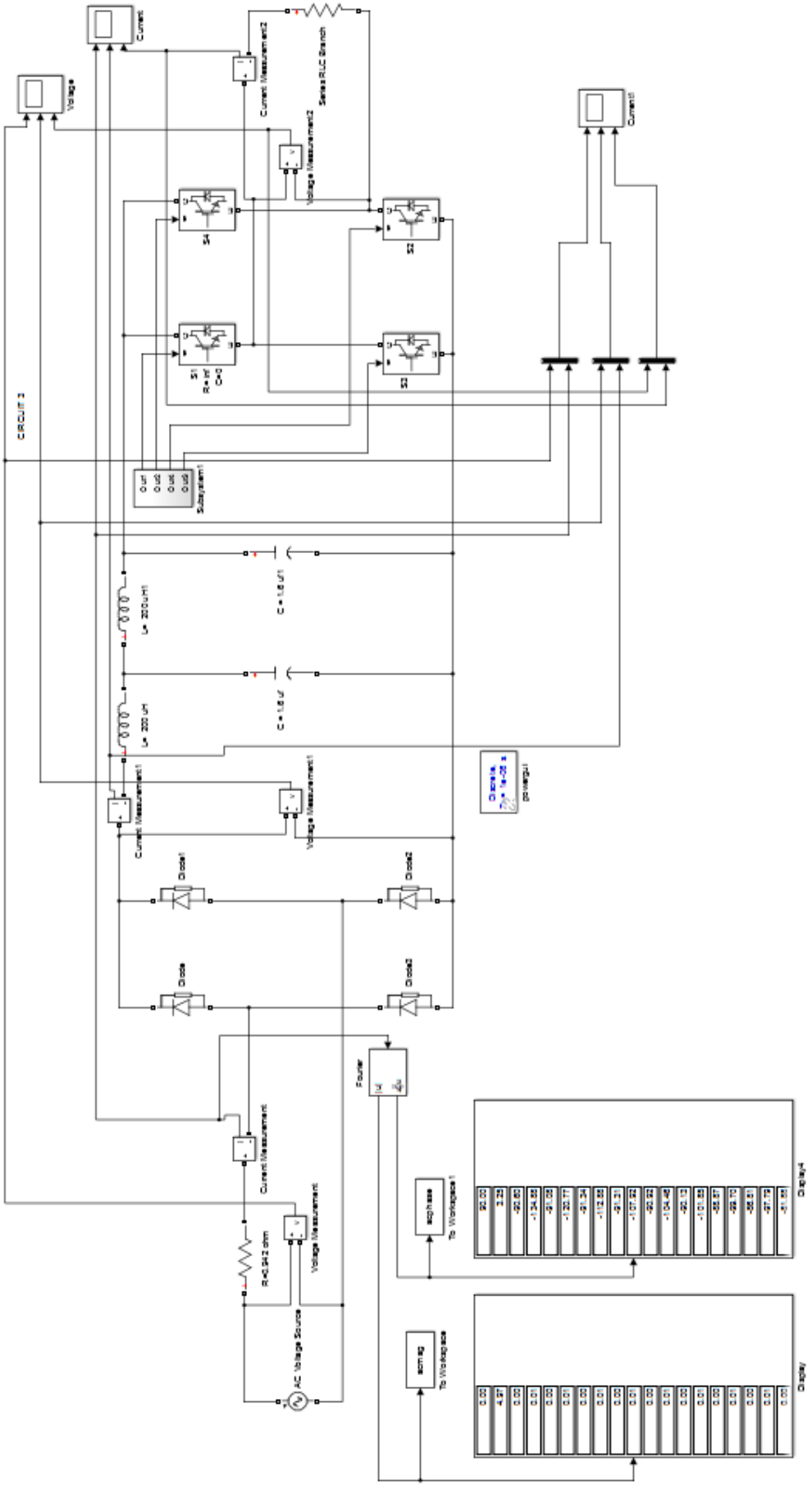


FIGURE 7.19: MATLAB simulation model.

After conducting the detailed simulation with all the data, a harmonic analysis was conducted, which was done at various duty cycles from 25% to 95% with 5% increments.

Simulation result at 25% duty-cycle is shown in Figures 7.20 to 7.22.

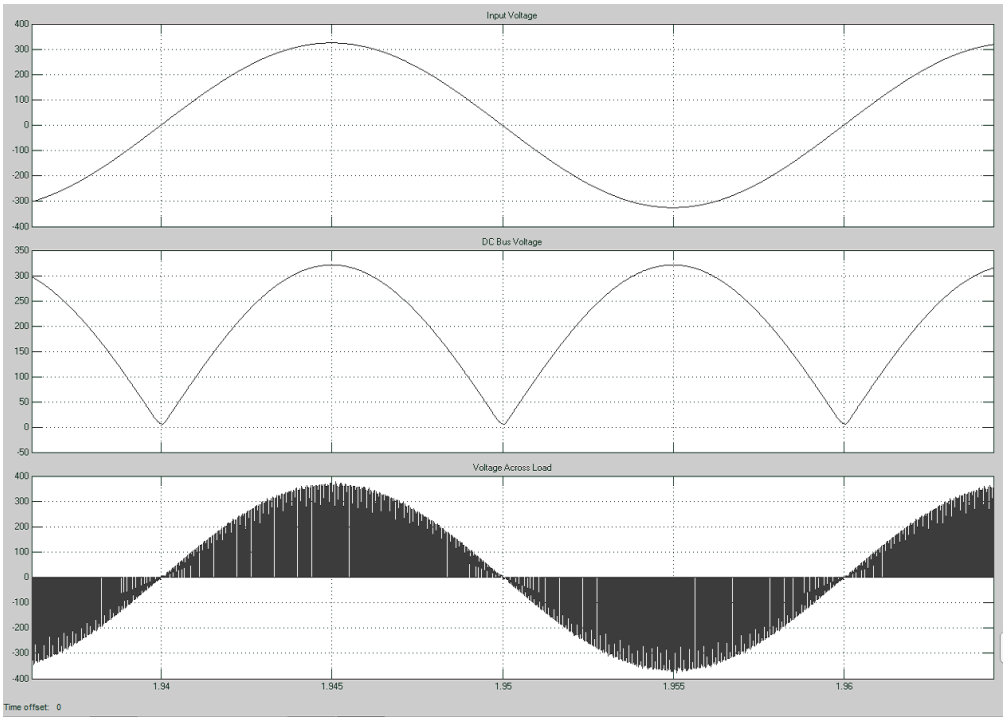


FIGURE 7.20: Voltage waveform at 25% duty-cycle

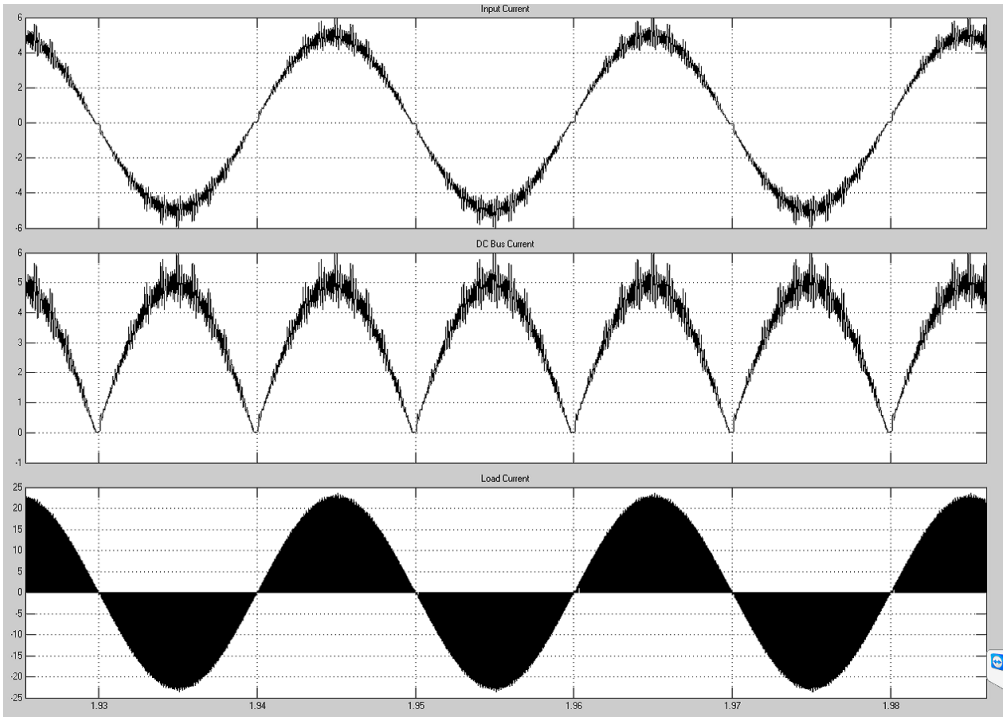


FIGURE 7.21: Current waveform at 25% duty-cycle

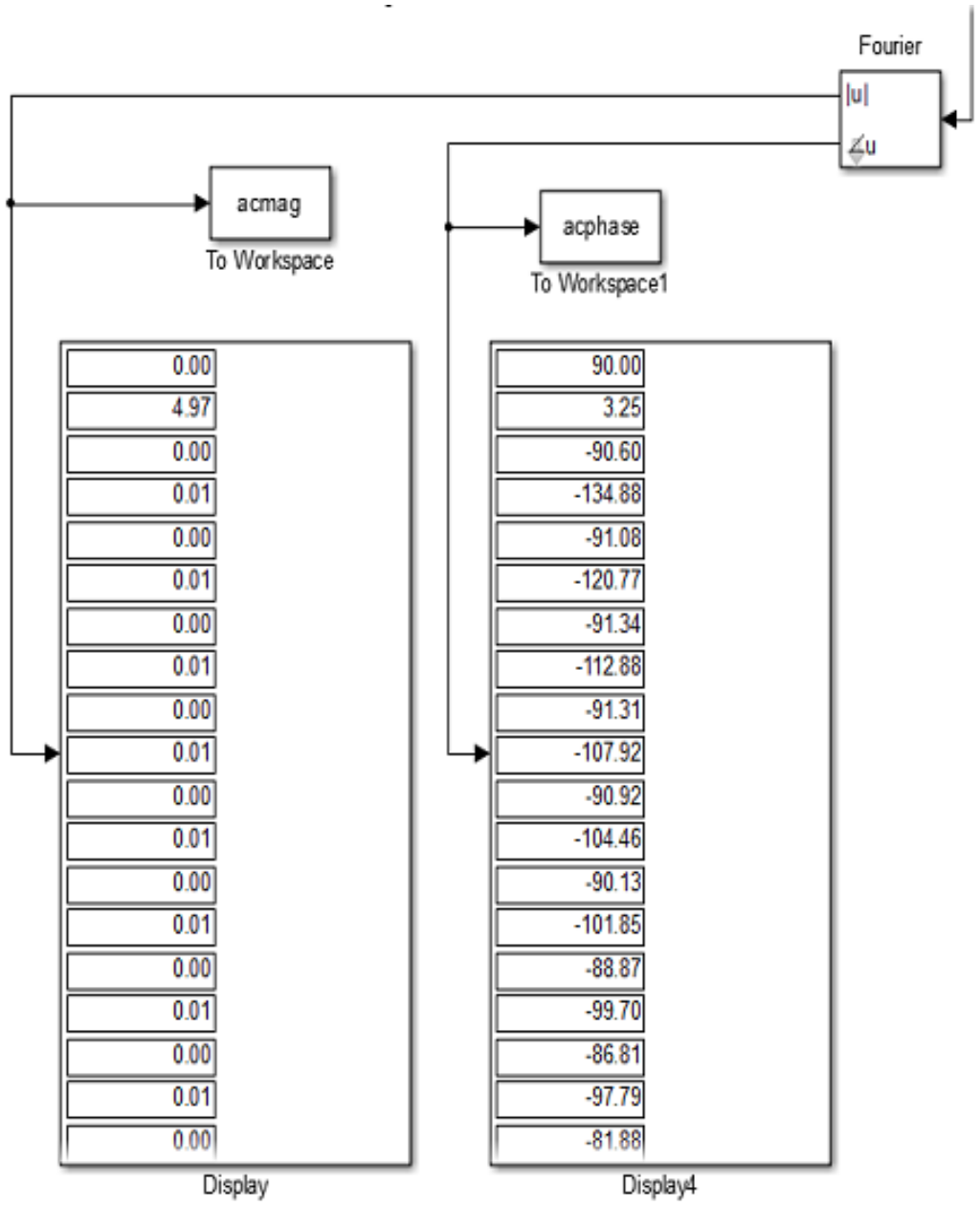


FIGURE 7.22: Harmonic current values at 25% duty-cycle

Figures 7.24 to 7.25 shows simulation result of model at 25% duty-cycle

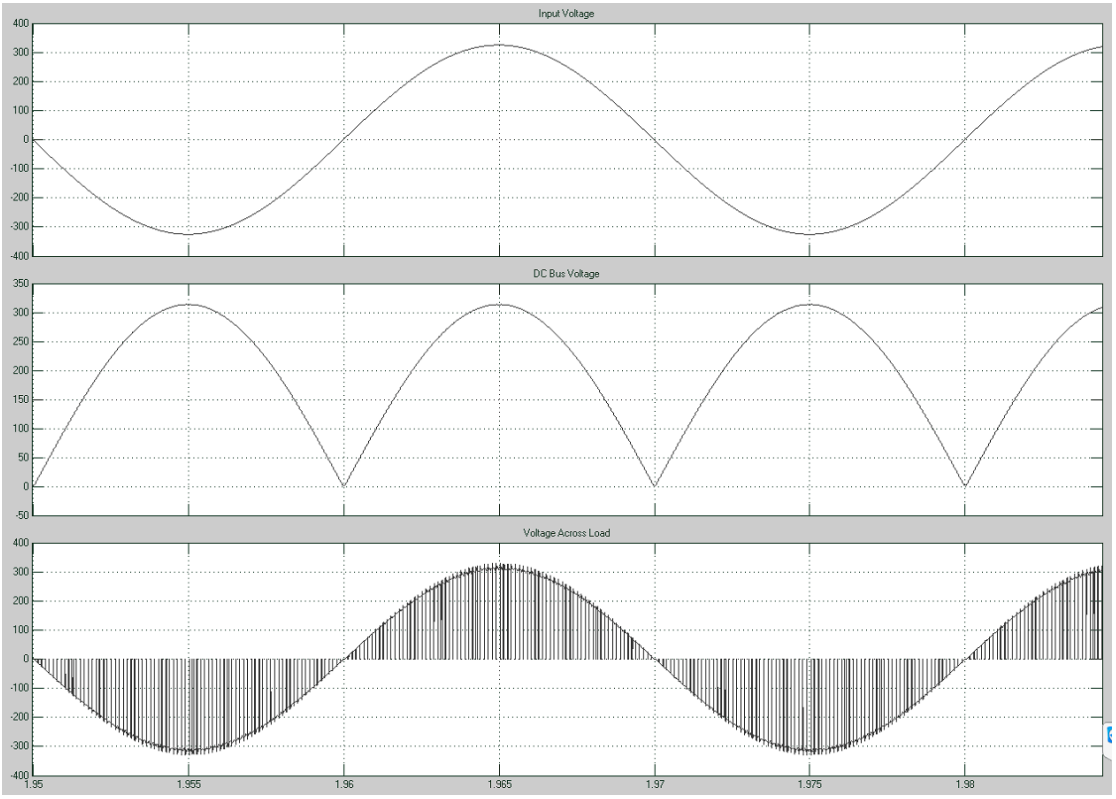


FIGURE 7.23: Voltage waveform at 95% duty-cycle

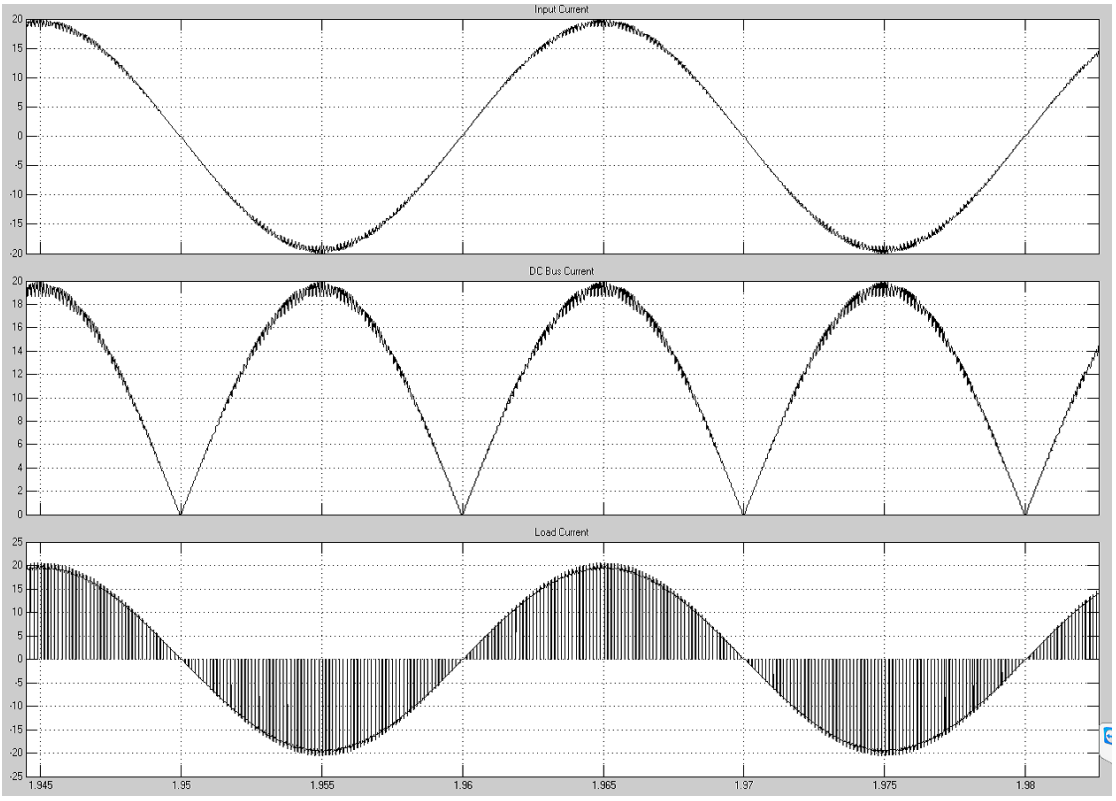


FIGURE 7.24: Current waveform at 95% duty-cycle

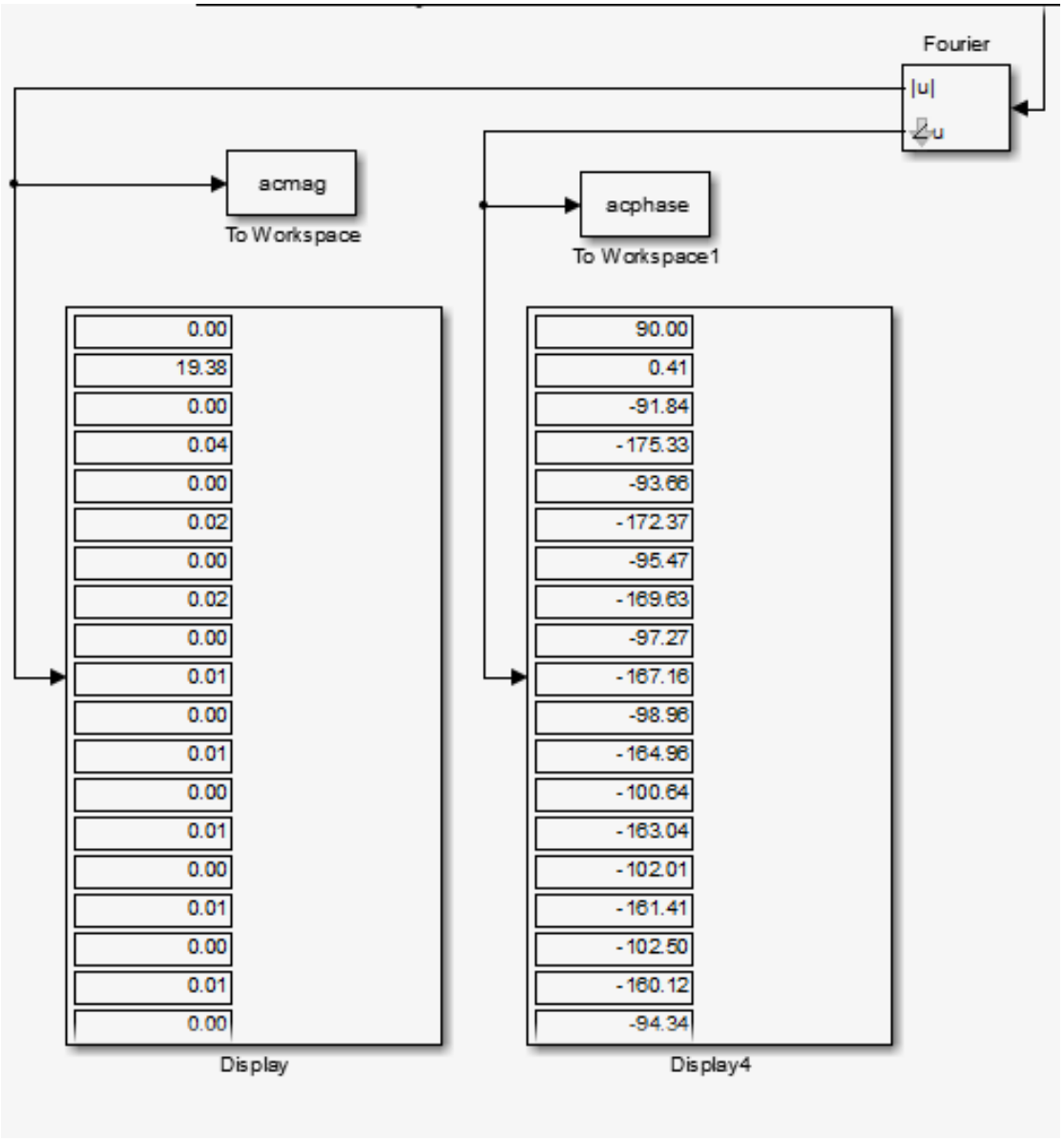


FIGURE 7.25: Harmonic current values at 95% duty-cycle

Figure 7.20 to 7.25 show the result of MATLab simulation at 95% duty cycle. They clearly show that continuous rectifier conduction is maintained, and the DC bus voltage follows the wave form of a rectified sinisoid. This ensures that harmonics currents on the AC side are mainly limmited to those around multifles of the switching frequency, and lower order harmonics are all but eliminated.

Chapter 8

Conclusion

8.1 Summary

This thesis is a document on the development of a Smart Domestic Water Heater Controller which in future could be integrated to existing electric power grid. The SDWHC would help in increasing the grid performance by using domestic water heaters as a reserve to be used in an event of faults in the AC system. The present grid system, its operation and methods which govern the voltage and frequency were discussed as background information. The specification according to the system requirement and New Zealand standards were detailed in system specification. The design procedures of electrical, mechanical and PCB design were detailed in later stages of the thesis.

Finally, the test result of the circuit and detailed simulation results according to revised prototype model were studied. The test result along with background data suggests that SDWHC can be effectively employed to control the reserves discussed in Chapter 2. SDWHC could control the load more effectively than the ripple control, since SDWHC monitors the grid parameters in real time whereas the ripple control relies on the ripple signal from the distribution company to disconnect the domestic water heater load. The hardware demonstrates that it is practical to use domestic water heater loads to help control the system voltage and frequency.

Thus extending their use to more intelligent and fast-operating demand-side management. This sort of device heralds a new era in the participation of loads in maintaining stable, reliable and cost effective electric power systems.

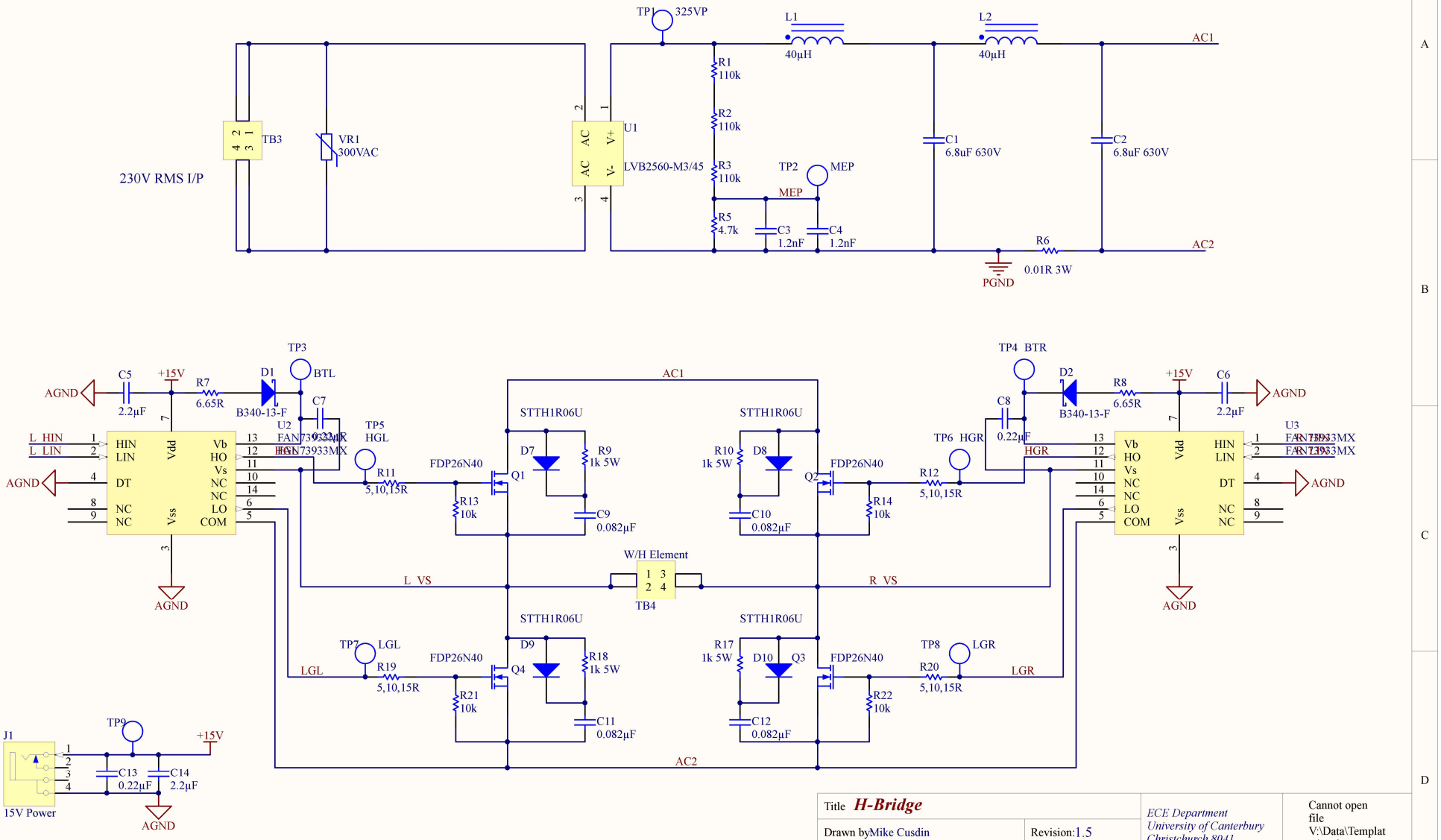
8.2 Future Prospects

Domestic devices that actively respond to global system frequency or local voltage levels do not exist, and there is no market structure to incentive their use. Quite a bit of whole is required to design a system that can attribute an appropriate value to this service. Futher functionality could be added via a communication link, which could allow

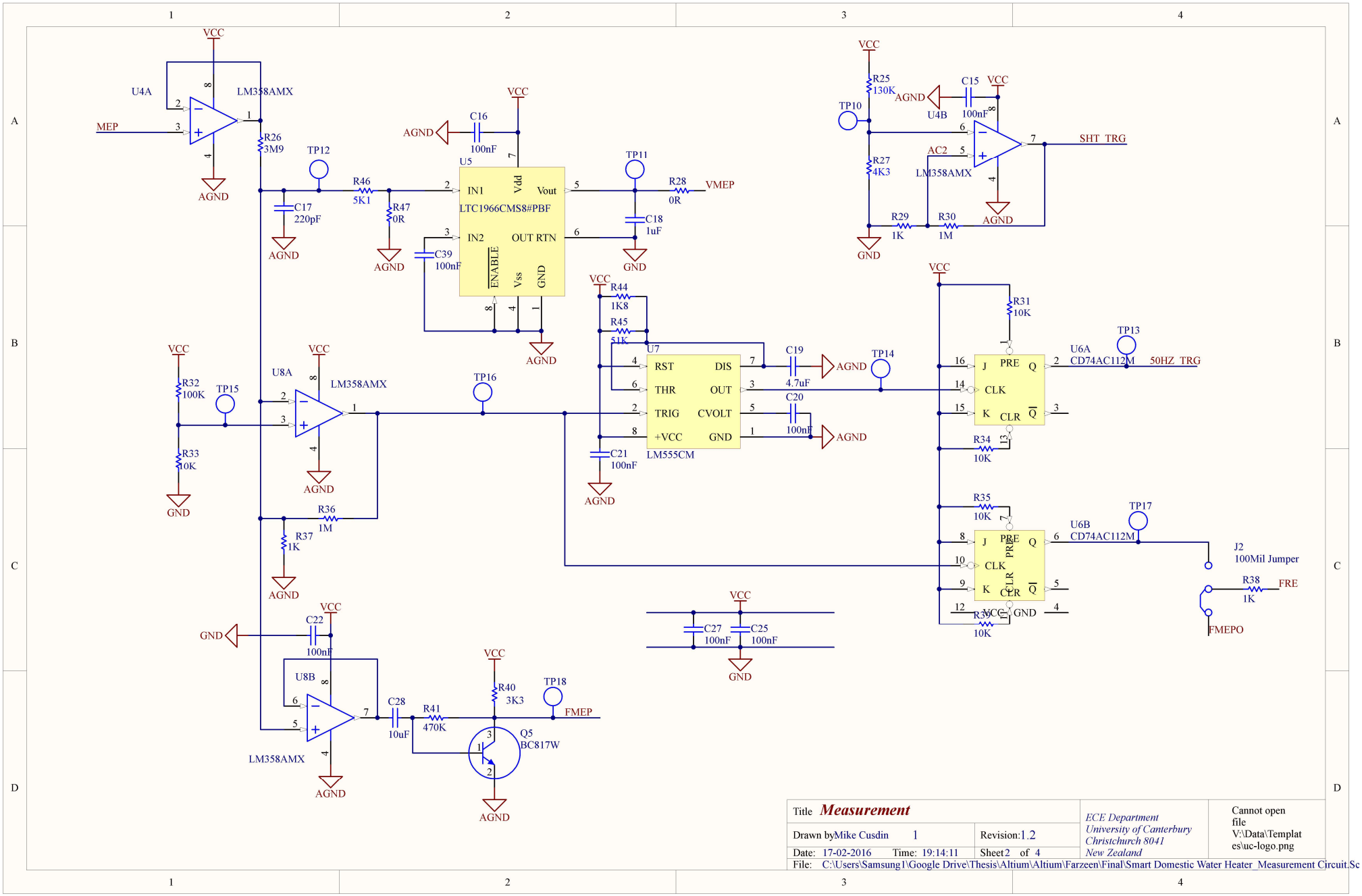
1. Determine energy use pattern.
2. Schedule the load according to generation pattern.
3. In future when more renewables are being integrated in to the system, SDWHC can help study the local generation pattern.

Appendix A

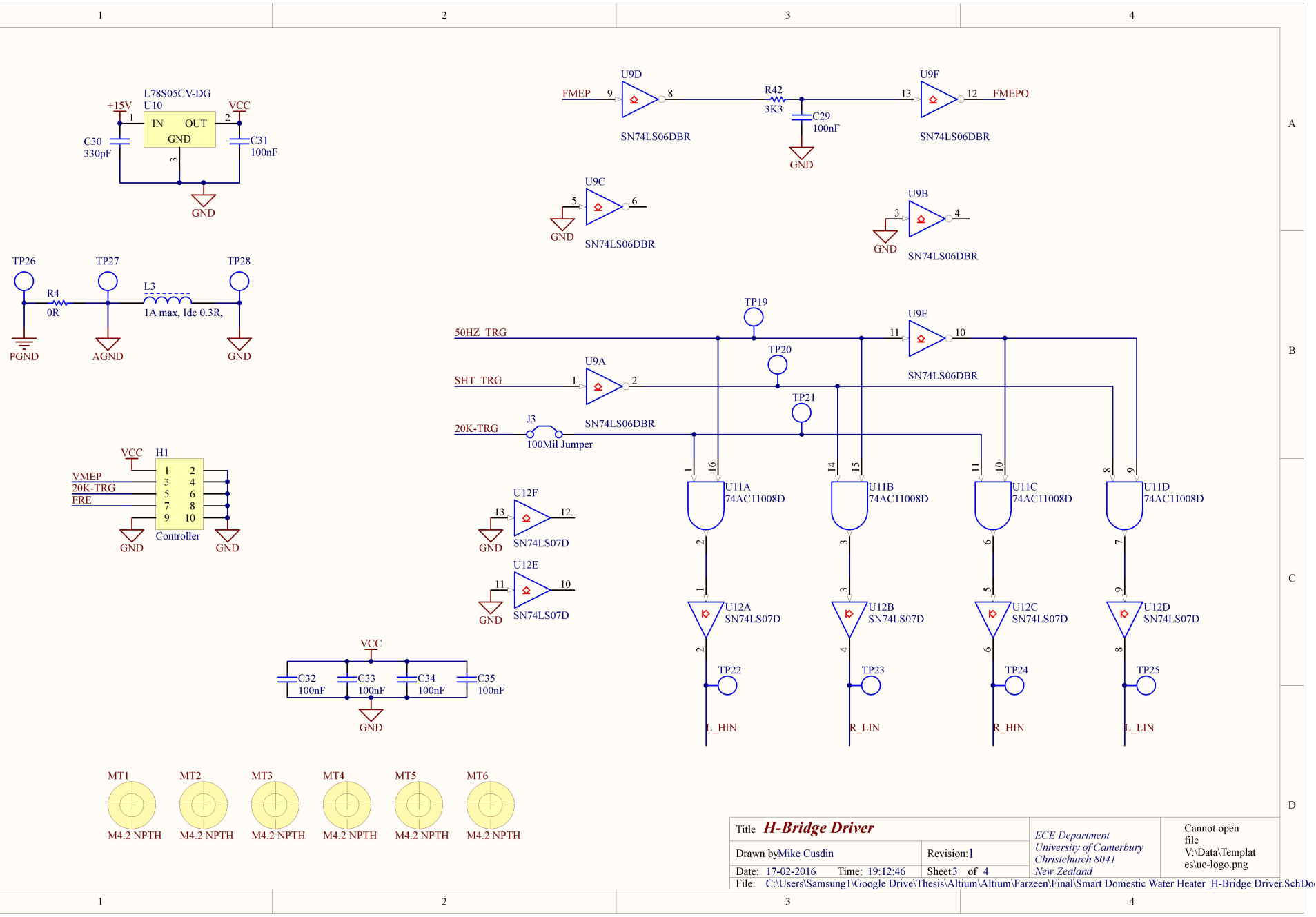
Smart Domestic Hot Water Heater Controller Circuit Diagram and PCB Layout



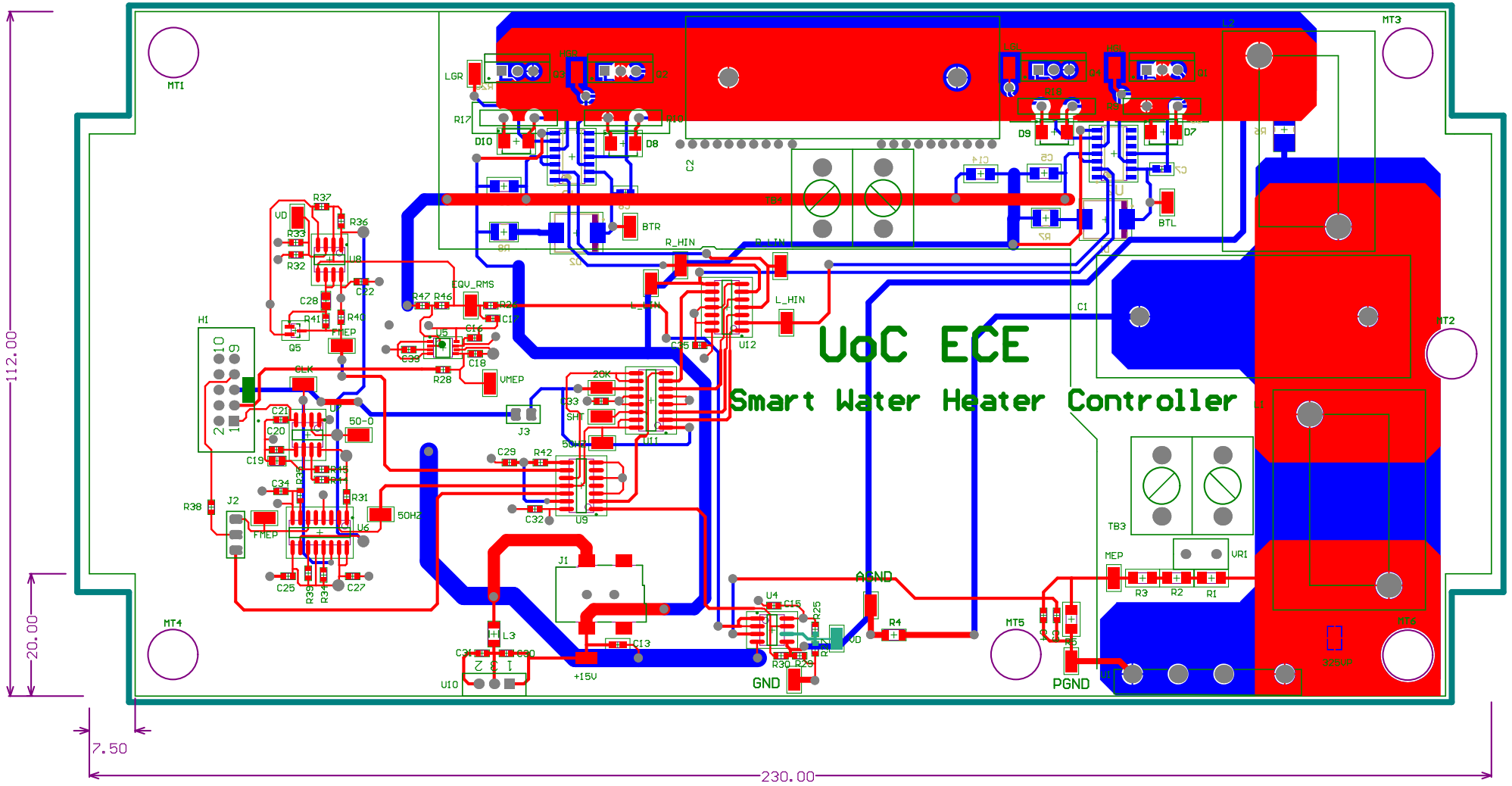
Title **H-Bridge**		*ECE Department* *University of Canterbury* *Christchurch 8041* *New Zealand*	Cannot open file V:\Data\Templates\uc-logo.png
Drawn by Mike Cusdin	Revision: 1.5		
Date: 17-02-2016 Time: 19:13:22	Sheet 1 of 4		
File: C:\Users\Samsung1\Google Drive\Thesis\Altium\Altium\Farzeen\Final\Smart Domestic Water Heater_H-Bridge.SchDoc			

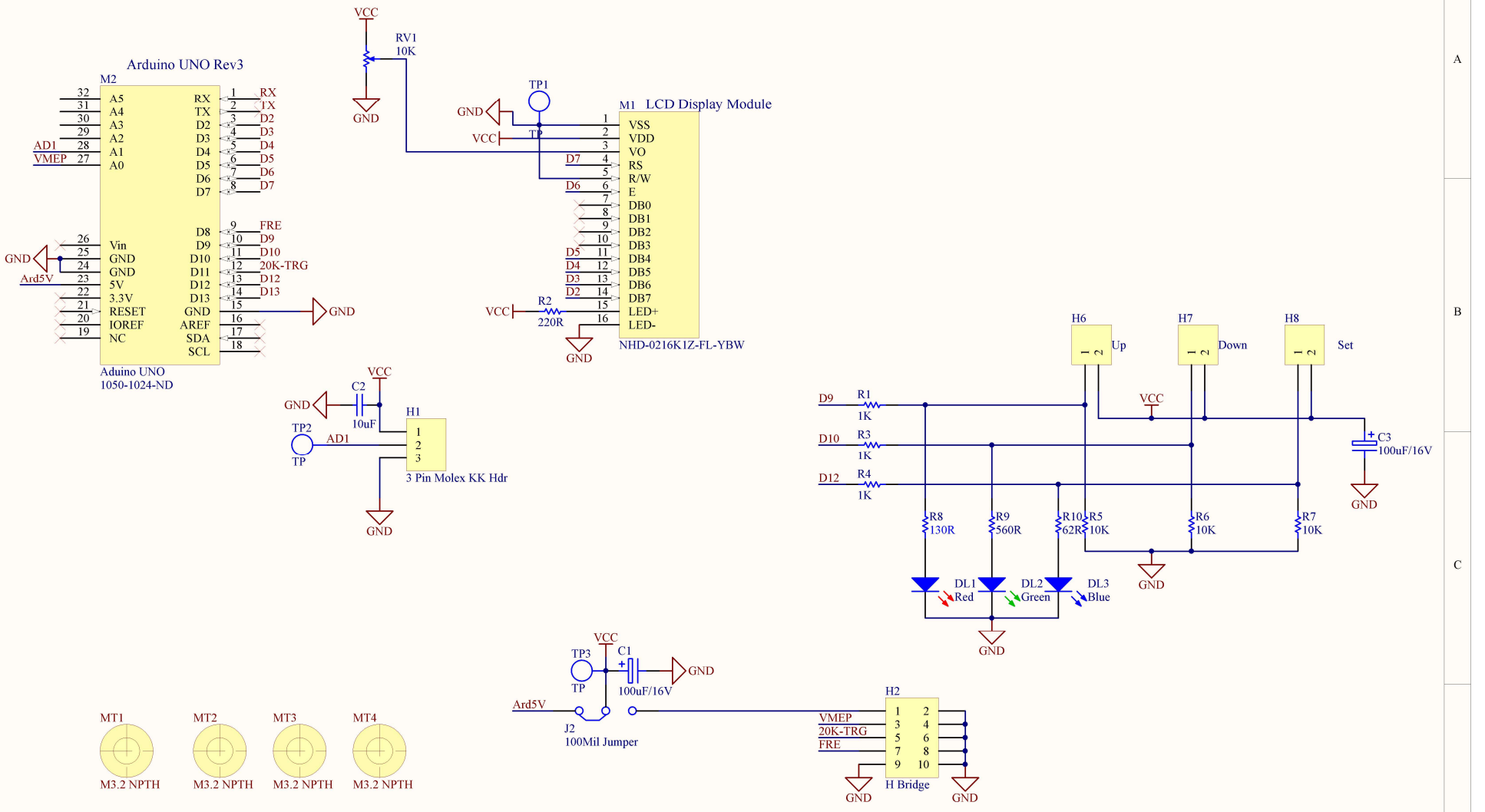


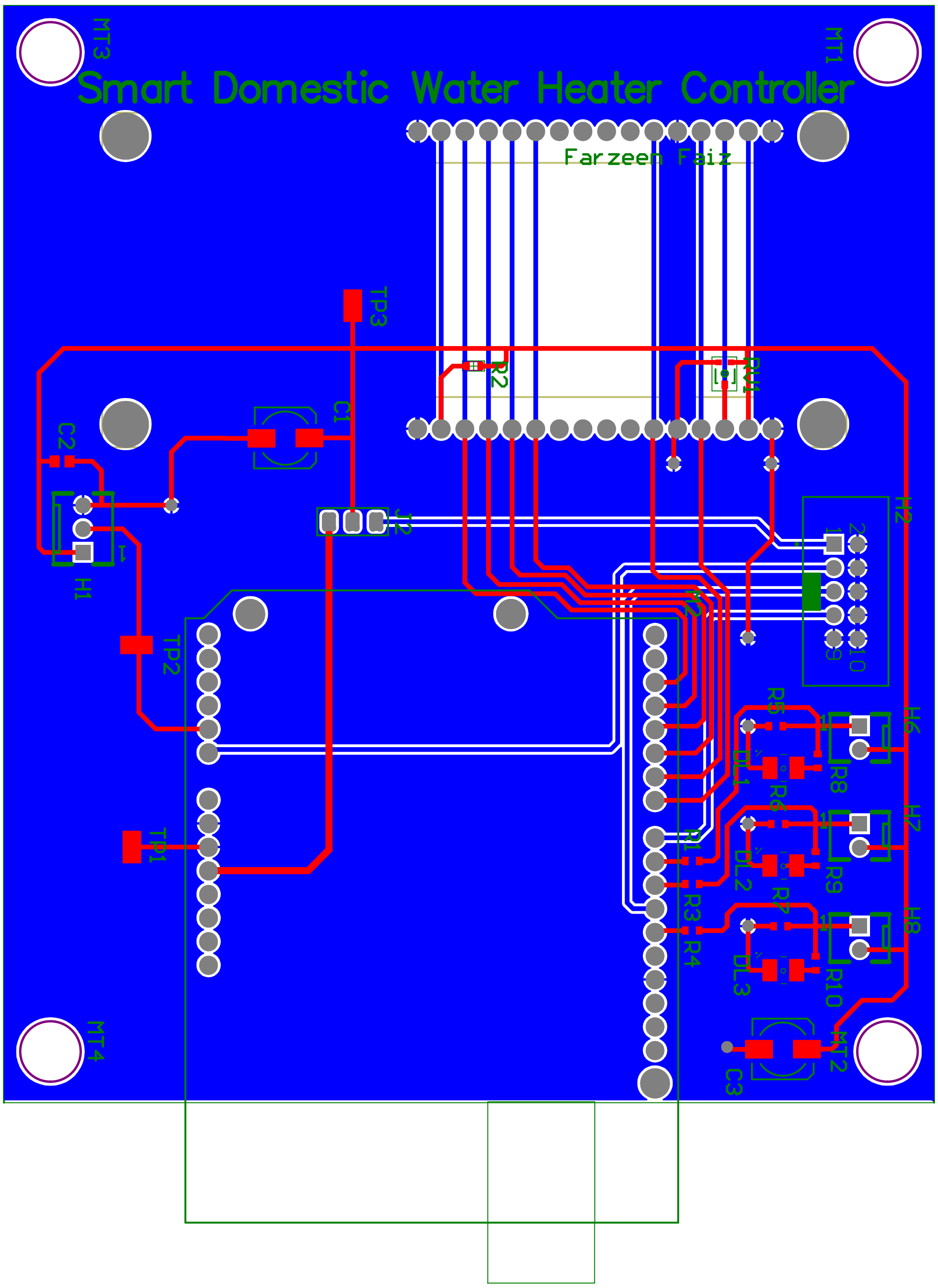
Title **Measurement**		*ECE Department*	Cannot open file V:\Data\Templates\uc-logo.png
Drawn by Mike Cusdin 1	Revision: 1.2	*University of Canterbury*	
Date: 17-02-2016 Time: 19:14:11	Sheet 2 of 4	*Christchurch 8041*	
File: C:\Users\Samsung1\Google Drive\Thesis\Altium\Altium\Farzeen\Final\Smart Domestic Water Heater_Measurement Circuit.Sc		*New Zealand*	



Title **H-Bridge Driver**		*ECE Department* *University of Canterbury* *Christchurch 8041* *New Zealand*	Cannot open file V:\Data\Templates\uc-logo.png
Drawn by Mike Cusdin	Revision: 1		
Date: 17-02-2016 Time: 19:12:46	Sheet 3 of 4		
File: C:\Users\Samsung1\Google Drive\Thesis\Altium\Altium\Farzeen\Final\Smart Domestic Water Heater_H-Bridge Driver.SchDoc			


UoC ECE
Smart Water Heater Controller
112.00
20.00
7.50
230.00
MT1
MT2
MT3
MT4
MT5
MT6
AGND
GND
PGND
+15V
LGR
LGL
HGR
HGL
BTR
BTL
R_HIN
L_HIN
EQU_RMS
VMEP
IMEP
VRI
IRI
MEP
50HZ
TB3
TB4
H1
J1
J2
J3
U1
U4
U5
U6
U8
U9
U10
U11
U12
Q5
D7
D8
D9
D10
C1
C2
L1
L2
L3
R1
R2
R3
R4
R5
R17
R28
R31
R36
R37
R38
R42
R46
R47
20K
50K
SHT
325VP


Arduino UNO Rev3
M2
Aduino UNO
1050-1024-ND
M1 LCD Display Module
NHD-0216K1Z-FL-YBW
RV1
10K
TP1
R2
220R
C2
10uF
H1
3 Pin Molex KK Hdr
TP2
H6
Up
H7
Down
H8
Set
R1
1K
R3
1K
R4
1K
C3
100uF/16V
R8
130R
R9
560R
R10
62R
R5
10K
R6
10K
R7
10K
DL1
Red
DL2
Green
DL3
Blue
TP3
C1
100uF/16V
J2
100Mil Jumper
H2
H Bridge
MT1
MT2
MT3
MT4
M3.2 NPTH
VCC
GND
Ard5V
AD1
VMEP
20K-TRG
FRE
Title Smart Domestic Water Heater Controller
Drawn by Mike Cusdin
Revision: 2
Date: 18-02-2016 Time: 09:11:45
Sheet 1 of 1
ECE Department
University of Canterbury
Christchurch 8041
New Zealand
Cannot open file V:\Data\Templates\uc-logo.png
File: C:\Users\Samsung1\Google Drive\Thesis\Altium\Altium\Farzeen\Smart Domestic Water Heater Controller\Smart Domestic Wa


Smart Domestic Water Heater Controller
Farzeen Faiz
MT1
MT2
MT3
MT4
TP1
TP2
TP3
C1
C2
C3
H1
H2
H6
H7
H8
J2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
RV1
DL1
DL2
DL3

Appendix B

Processor Program

```
#include<LiquidCrystal.h>          //Header file for including lcd functions.
#include<FreqMeasure.h>            //Header file for including frequency measurement functio
LiquidCrystal lcd(7,6,5,4,3,2);    //Assigning ports to connect lcd.

float fre;                         //Setting frequency measurement pin to digital pin 8
int up=9;                          //Setting increment pin to digital pin 9
int dn=10;                         //Setting decrement pin to digital pin 10
int set=12;                        //Set pin to digital pin 12
int v1=210;                        //Minimum cut off voltage.
int v2=240;                        //Maximum cut off voltage.
float vlt;                           //Variable for measured voltage
float f1=48;                       //Minimum cut-off frequency
float f2=49;                       //Intermediate frequency
float f3=51;                       //Maximum cut-off frequency
float dcv=25;                      //Duty cycle corresponding to voltage profile
float dcf=50;                      //Duty cycle corresponding to frequency profile
float dc;                          //Duty cycle
double sum=0;                     //variable for frequency measurement
int count=0;                      //variable for frequency measurement
//A0 = RMS Check
// A1 = Temperature Check
void limitset();                           // Function for limit setting
float settng(float,float,float,float);     // Function for frequency setting mechanism
float fremeasure();                        // Function for frequency measurement
float vltmeasure();                        // Function for voltage measurement
int fndcv(float);                          // Function for DC corresponding to voltage
int fndcf(float);                          // Function for DC corresponding to frequency

void setup() {
int stime;                         //Initial time setting
int flag;                          //Flag for breaking loop when flag=1,Break
lcd.begin(16,2);
FreqMeasure.begin();
digitalWrite(11,LOW);
Serial.begin(9600);
Serial.println("Default Parameters");
Serial.print("Minimum frequency:");
```

```
Serial.println(f1);
Serial.print("Intermediate frequency:");
Serial.println(f2);
Serial.print("Maximum frequency:");
Serial.println(f3);
Serial.print("Duty Cycle frequency profile:");
Serial.println(dcf);
Serial.print("Minimum Voltage:");
Serial.println(v1);
Serial.print("Maximum Voltage:");
Serial.println(v2);
Serial.print("Duty Cycle voltage profile:");
Serial.println(dcv);
Serial.println("*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*");
delay(1000);
pinMode(up,INPUT);
pinMode(dn,INPUT);
pinMode(set,INPUT);
stime=0;
flag=0;
do
{
    int s=digitalRead(set);
    if(s=1)
    {
    flag=1;
    limitset();
}
if(flag==1)
break;
stime++;
delay(100);
}while(stime<60);
Serial.println("set Parameters");
Serial.print("Minimum frequency:");
Serial.println(f1);
Serial.print("Intermediate frequency:");
Serial.println(f2);
Serial.print("Maximum frequency:");
Serial.println(f3);
Serial.print("Duty Cycle frequency profile:");
Serial.println(dcf);
Serial.print("Minimum Voltage:");
Serial.println(v1);
Serial.print("Maximum Voltage:");
Serial.println(v2);
Serial.print("Duty Cycle voltage profile:");
Serial.println(dcv);
```

```
86 delay(1000);
87 }
88
89
90 void loop() {
91 // put your main code here, to run repeatedly:
92 int dc1,dc2;
93 int temp,flag;
94 flag=0;
95 temp=analogRead(A1);
96 temp=map(temp,0,1024,0,100);  //Mapping the measured temperature
97 if(temp>=60)
98     if(temp>=70)
99     flag=1;
100 vlt=vltmeasure();
101 Serial.print("voltage");
102 Serial.println(vlt);
103 if (FreqMeasure.available()) {
104 // average several reading together
105 sum = sum + FreqMeasure.read();
106 count = count + 1;
107     if (count > 30)
108     {
109         float frequency = FreqMeasure.countToFrequency(sum / count);
110         Serial.println(frequency);
111         fre=frequency;
112         sum = 0;
113         count = 0;
114     }
115 }
116 Serial.print("Frequency");
117 Serial.println(fre);
118 dc1=fndcv(vlt);
119 Serial.print("Duty cycle 1");
120 Serial.println(dc1);
121 dc2=fndcf(fre);
122 dc=((0.5*dc1)+0.5*dc2);
123 Serial.print("Duty cycle 2");
124 Serial.println(dc2);
125 if(flag>0)
126 analogWrite(11,dc2);
127 delay(50);
128 lcd.clear();
129 lcd.print("Success");
130 }
131
132 void limitset(){                              // Function for limit setting
133 lcd.clear();
```

```
134 lcd.setCursor(0,0);
135 lcd.print("Set Minimum Voltage:");
136 v1=setting(210,240,1,230);
137 
138 lcd.clear();
139 lcd.setCursor(0,0);
140 lcd.print("Set Maximum Voltage:");
141 v2=setting(210,240,1,230);
142 
143 lcd.clear();
144 lcd.setCursor(0,0);
145 lcd.print("Set DC Vlt pfl:");
146 dcv=setting(25,100,1,50);
147 
148 lcd.clear();
149 lcd.setCursor(0,0);
150 lcd.print("Set Minimum Frequency:");
151 f1=setting(48,51,0.1,50);
152 
153 lcd.clear();
154 lcd.setCursor(0,0);
155 lcd.print("Set Int Frequency:");
156 f2=setting(48,51,0.1,50);
157 
158 lcd.clear();
159 lcd.setCursor(0,0);
160 lcd.print("Set Maximum Frequency:");
161 f3=setting(48,51,0.1,50);
162 
163 lcd.clear();
164 lcd.setCursor(0,0);
165 lcd.print("Set DC Fre pfl:");
166 dcv=setting(25,100,1,50);
167 }
168 
169 float setting(float x1, float x2,float inc,float ref){                  // Function for volt
170 float  s;
171 float ref1=ref;
172 do
173 {
174     int u=digitalRead(up);
175     int d=digitalRead(dn);
176     if(u==1)
177     {
178         if(u==1&&ref1>=x2)
179         {
180             ref1=x1;
181         }
```

```
182         else
183         {
184             ref1+=inc;
185         }
186     }
187     if(d==1)
188     {
189         if(d==1&&ref1<=x1)
190         {
191             ref1=x2;
192         }
193         else
194         {
195             ref1-=inc;
196         }
197     }
198     lcd.setCursor(0,1);
199     lcd.print(ref1);
200     s=digitalRead(set);
201     delay(125);
202 }while(s<1);
203 return (ref1);
204 delay(200);
205 }
206 
207 float fremeasure(){      // Function for frequency measurement
208 if (FreqMeasure.available())
209 {  average several reading together
210 sum = sum + FreqMeasure.read();
211 count = count + 1;
212 if (count > 30)
213 {
214 float frequency = FreqMeasure.countToFrequency(sum / count);
215 Serial.println("frequency");
216 Serial.println(frequency);
217 return (frequency);
218 sum = 0;
219 count = 0;
220 }
221 }
222 }
223 
224 float vltmeasure(){        // Function for voltage measurement
225 
226 int x=analogRead(A0);
227 float mvlt=0;
228 for(int i=0;i<10;i++)
229 {
```

```
230 int y=map(x,0,1024,0,250);
231 mvlt+=y;
232 delay(50);
233 }
234 return (mvlt/10);
235 }
236
237 int fndcv( float vl1)
238 {
239 int x,x1;
240 if(vl1>v2)
241 x=100;
242 else if(vl1>=v1&&vl1<=v2)
243 {
244 x=(((100-dcv)*(vl1-v1))/(v2-v1))+dcv;
245 }
246 else if(vl1<v1)
247 x=0;
248 x1=map(x,0,100,0,225);
249 return (x1);
250 }
251
252 int fndcf( float fr1)
253 {
254 int x,x1;
255 float frl;
256 if(fr1<f1)
257 x=0;
258 else if(fr1>=f1&& fr1<f2)
259 {
260 x=((dcf*(fr1-f1))/(f2-f1));
261 }
262 else if(fr1>=f2&&fr1<=f3)
263 {
264 x=(((100-dcf)*(frl-f2))/(f3-f2))+dcf;
265 }
266
267 else if(fr1>f3)
268 x=100;
269
270 x1=map(x,0,100,0,225);
271 return(x1);
272 }
```

Appendix C

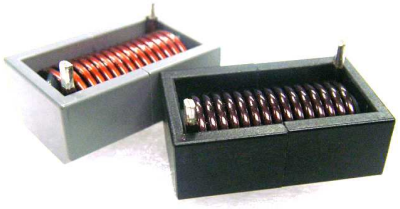
Data Sheets

TT electronics

Electrical / Environmental

HA55

Power Inductor

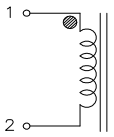


NEW

RoHS Compliant

- Operating Temperature Range -40℃ to +155℃
- Ambient Temperature, Maximum +85℃
- High inductance, high efficiency and excellent current handling.
- Use as DC-DC converter and in high current applications. Suitable for industrial as well as automotive application.

Electrical Schematic



Specifications @ 25℃

Part Number	INDUCTANCE 100kHz, 100mV (µH) TYP	@RATED CURRENT INDUCTANCE 100kHz, 100mV (µH) TYP	I_{rated} RATED CURRENT (A)	I_{sat} SATURATION CURRENT (A)	DC Resistance mΩ Typ	DC Resistance mΩ Max	FIGURE
HA55-3623200LF	20.00	14.50	33.00	35.0	3.35	3.85	1
HA55-3023115LF	11.50	8.24	39.00	43.0	2.30	2.76	2
HA55-2223070LF	7.00	5.33	40.00	48.0	1.70	2.00	3
HA55-3023130LF	13.00	9.33	37.00	40.0	2.50	3.25	4
HA55L-3623220LF*	22.00	13.00	34.00	26.0	3.35	3.85	1
HA55L-3023135LF*	13.50	8.42	39.00	30.0	2.30	2.76	2
HA55L-2223088LF*	8.83	5.52	41.00	33.0	1.70	2.00	3
HA55L-3023163LF*	16.30	9.38	37.00	27.0	2.50	3.25	4
HA55L-3623400LF*	40.00	24.00	26.00	20.0	5.70	6.20	1
HA55L-4523500LF*	50.00	26.00	32.00	20.0	7.25	8.35	5

Notes :

(1) Inductance is measured at 100kHz, 0.1Vrms, 0Adc.

(2) The rated current is the approximate DC current at which ΔT is approximately 60℃. This current is determined by soldering the unit on a typical application PCB, and then applying the current to the unit for 30 minutes.

(3) Isat is the saturation current at which inductance rolls off approximately 30% from its initial unbias inductance value.

* Low cost version

BI technologies
www.bitechnologies.com

wakefield-vette

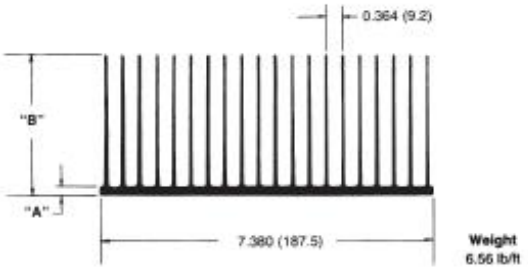
Standard Catalog P/N[5]				Height		Thermal Resistance [5] (Øsa) at Typical Load	
Milled Base[1]	Nonmilled Base[2]	Base Width in. (mm)	Length in. (mm)	Milled Base [1] ("M Series") in. (mm)	Nonmilled Base [2] ("U" Series) in. (mm)	Natural Convection[3] (°C/W)	Forced Convection[4] (°C/W @ 100 CFM)
510-3M	510-3U	7.380 (187.452)	3.000 (76.2)	3.106 (78.9)	3.136 (79.7)	0.56	0.088
510-6M	510-6U	7.380 (187.452)	6.000 (152.4)	3.106 (78.9)	3.136 (79.7)	0.38	0.070
510-9M	510-9U	7.380 (187.452)	9.000 (228.6)	3.106 (78.9)	3.136 (79.7)	0.29	0.066
510-12M	510-12U	7.380 (187.452)	12.000 (304.8)	3.106 (78.9)	3.136 (79.7)	0.24	0.062
510-14M	510-14U	7.380 (187.452)	14.000 (355.6)	3.106 (78.9)	3.136 (79.7)	0.21	0.059
511-3M	511-3U	5.210 (132.33)	3.000 (76.2)	2.350 (59.7)	2.410 (61.2)	0.90	0.120
511-6M	511-6U	5.210 (132.33)	6.000 (152.4)	2,350 (59.7)	2.410 (61.2)	0.65	0.068
511-9M	511-9U	5.210 (132.33)	9.000 (228.6)	2.350 (59.7)	2.410 (61.2)	0.56	0.060
511-12M	511-12U	5.210 (132.33)	12.000 (304.8)	2.350 (59.7)	2.410 (61.2)	0.45	0.045
512-3M	512-3U	7.200 (182.88)	3.000 (76.2)	2.350 (59.7)	2.410 (61.2)	0.90	0.120
512-6M	512-6U	7.200 (182.88)	6.000 (152.4)	2.350 (59.7)	2.410 (61.2)	0.65	0.068
512-9M	512-9U	7.200 (182.88)	9.000 (228.6)	2.350 (59.7)	2.410 (61.2)	0.56	0.060
512-12M	512-12U	7.200 (182.88)	12.000 (304.8)	2.350 (59.7)	2.410 (61.2)	0.45	0.045

MECHANICAL DIMENSIONS

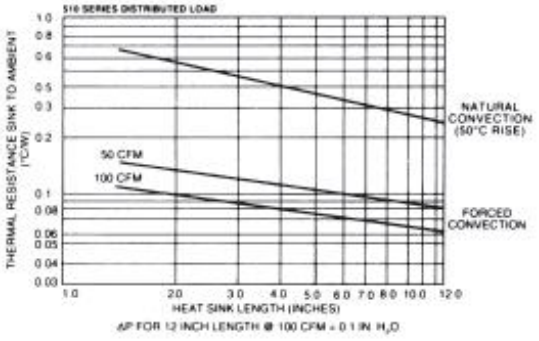
510 SERIES

510 Series (Extrusion Profile 5113)

Series	A	B	Flatness
510-U	0.216 (5.5)	3.136 (79.7)	0.006 in./in. (0.15 mm/mm)
510-M	0.165 (4.2)	3.106 (78.9)	0.002 in./in. (0.05 mm/mm)



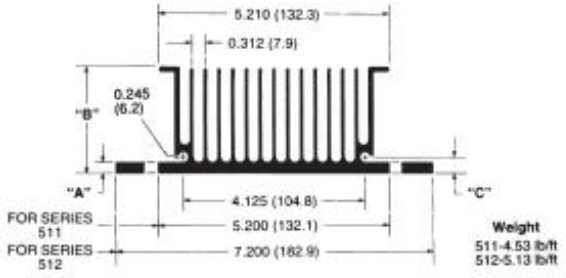
NATURAL AND FORCED CONVECTION CHARACTERISTICS

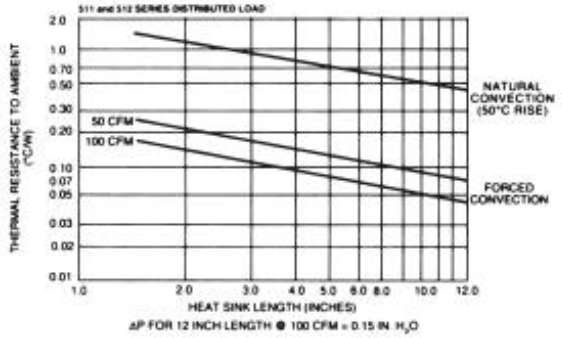


511 AND 512 SERIES

511 Series (Extrusion Profile 6438-1)
512 Series (Extrusion Profile 6438-2)

Series	A	B	C	Flatness
511-U 512-U	0.250 (6.4)	2.410 (61.2)	0.372 (9.4)	0.006 in./in. (0.15 mm/mm)
511-M 512-M	0.220 (5.6)	2.350 (59.7	0.342 (8.7)	0.002 in./in. (0.05 mm/mm)





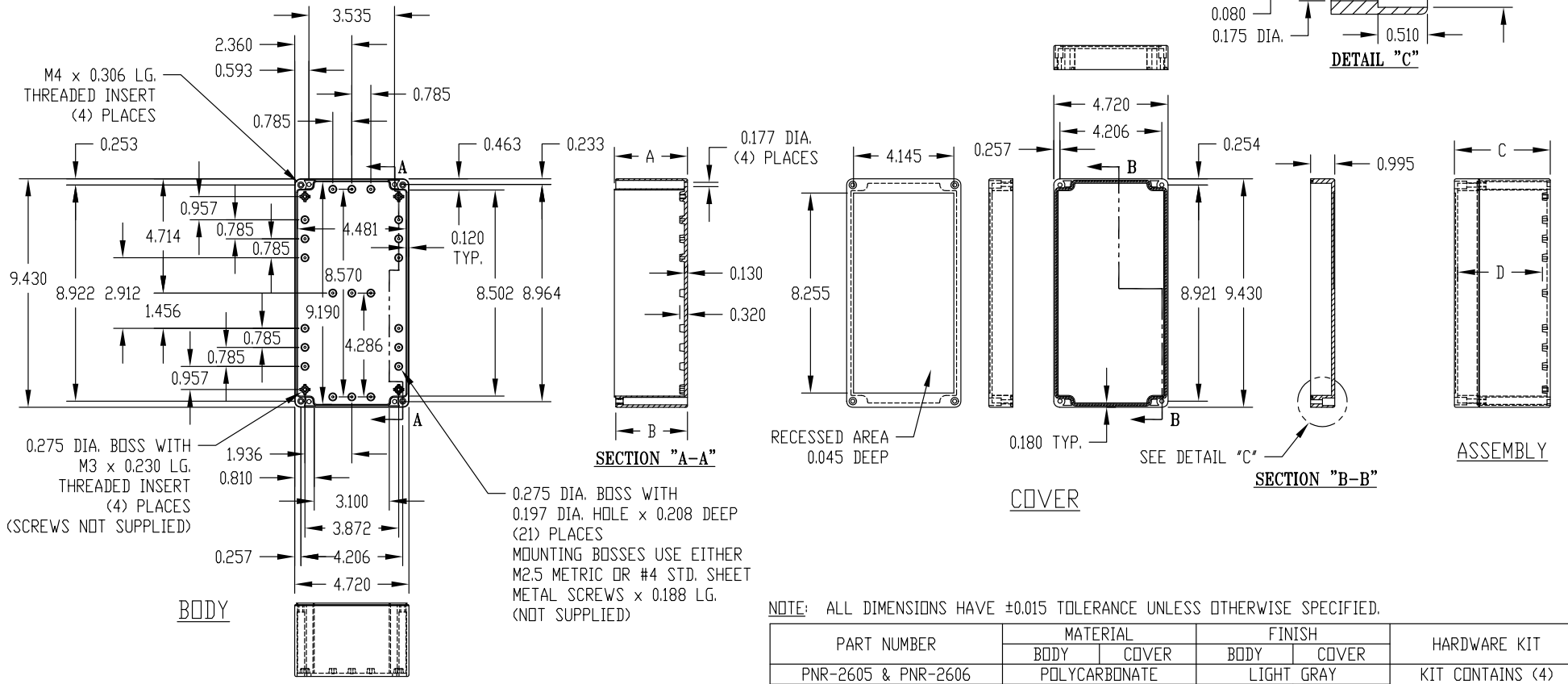
PART NAME	NEMA 4X ENCLOSURE	PART No.	PNR-2605, PNR-2605-C AND PNR-2605-DG PNR-2606, PNR-2606-C AND PNR-2606-DG	REV. DATE	11-17-08

INDUSTRY STANDARDS:

POLYCARBONATE (LIGHT GRAY AND CLEAR)
- UL94-HB FLAMMABILITY RATING (UL FILE #E41613)
- UV STABILIZED
- SERVICE TEMPERATURE RANGE: -40°C TO +120°C

ABS (DARK GRAY)
- UL94-HB FLAMMABILITY RATING (UL FILE #E56070)
- SERVICE TEMPERATURE RANGE: -40°C TO +80°C

PART NUMBER	DIMENSION			
	A	B	C	D
PNR-2605, PNR-2605-C AND PNR-2605-DG	1.442	1.382	2.377	1.926
PNR-2606, PNR-2606-C AND PNR-2606-DG	3.022	2.962	3.957	3.506



NOTE: ALL DIMENSIONS HAVE ±0.015 TOLERANCE UNLESS OTHERWISE SPECIFIED.

PART NUMBER	MATERIAL		FINISH		HARDWARE KIT
	BODY	COVER	BODY	COVER	
PNR-2605 & PNR-2606	POLYCARBONATE		LIGHT GRAY		KIT CONTAINS (4) M4 x 17mm (0.668") LG. SCREWS FOR ASSEMBLY
PNR-2605-C & PNR-2606-C	POLYCARBONATE		LIGHT GRAY	CLEAR	
PNR-2605-DG & PNR-2606-DG	HIGH-IMPACT ABS		DARK GRAY		

September 2014

LM78XX / LM78XXA
3-Terminal 1 A Positive Voltage Regulator

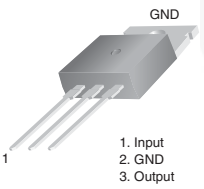
Features

- Output Current up to 1 A
- Output Voltages: 5, 6, 8, 9, 10, 12, 15, 18, 24 V
- Thermal Overload Protection
- Short-Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices can be used with external components for adjustable voltages and currents.

TO-220 (Single Gauge)



Ordering Information(1)

Product Number	Output Voltage Tolerance	Package	Operating Temperature	Packing Method
LM7805CT	±4%	TO-220 (Single Gauge)	-40°C to +125°C	Rail
LM7806CT				
LM7808CT				
LM7809CT				
LM7810CT				
LM7812CT				
LM7815CT				
LM7818CT				
LM7824CT				
LM7805ACT	±2%		0°C to +125°C	
LM7809ACT				
LM7810ACT				
LM7812ACT				
LM7815ACT				

Note:

1. Above output voltage tolerance is available at 25°C.

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